ensoniq®

ES 5506 "OTTO"

ENSONIQ Soundscape Wavetable Synthesizer

Revision 2.3

OTTO - ES5506

1 INTRODUCTION

OTTO is a VLSI device designed in a 1.5 micron double-metal CMOS process. The device is the next generation of audio technology from ENSONIQ. All calculations in the device are made with at least 18-bit accuracy. The major features of OTTO are:

- 68-PIN PLCC PACKAGE
- ON CHIP REAL TIME DIGITAL FILTERS
- FREQUENCY INTERPOLATION
- 32 INDEPENDENT VOICES
- LOOP START AND STOP POSITIONS FOR EACH VOICE
- BIDIRECTIONAL AND REVERSE LOOPING
- 68000 COMPATIBILITY FOR ASYNCHRONOUS BUS COMMUNICATION
- SEPARATE HOST AND SOUND MEMORY INTERFACE
- 6 CHANNEL STEREO SERIAL COMMUNICATION PORT
- PROGRAMMABLE CLOCKS FOR DEFINING SERIAL PROTOCOL
- INTERNAL VOLUME MULTIPLICATION AND STEREO PANNING
- A TO D INPUT FOR POTS AND WHEELS
- HARDWARE SUPPORT FOR ENVELOPES
- SUPPORT FOR DUAL OTTO SYSTEMS
- OPTIONAL COMPRESSED DATA FORMAT FOR SAMPLE DATA
- UP TO 16MHZ OPERATION

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1 THEORY OF OPERATION

OTTO is a sample playback synthesizer device. The main function of the chip is to play a specified area of memory and create a complete musical instrument through the on board signal processing. The OTTO Block diagram (page 4) illustrates the various sections of the chip and the overall signal flow. It will be useful to refer to this diagram during this discussion.

OTTO operates in a separate memory space called sound memory. The sound memory space can be up to 8 Megaword of 16-bit memory. The microprocessor communicates to OTTO through its 8-bit data bus and 6-bit address bus. OTTO contains thirty two independent voices each of which are controlled by twenty voice specific registers.

OTTO creates sound for each voice in succession by performing the following algorithm. The 21 bit integer portion of the 32-bit accumulator is placed on the Address Bus (A0 thru A20) along with a 2-bit bank select bits(BS1-0) to select a sample data word for memory. Each voice can address four 2 Megaword memory banks.

The sample data S1 is received from the Data Bus and placed in a temporary holding register. The address is then incremented by one and placed on the Address Bus. This sample, S2, is used with the previous sample, S1, to compute SF, the actual sample.

The value SF is now transferred to the filter computation section. In this section a real time 4-pole digital filter is implemented as four 1-pole filters cascaded in a chain. The first two poles are fixed as low pass filters the second two poles can be set independently as either high pass or low pass.

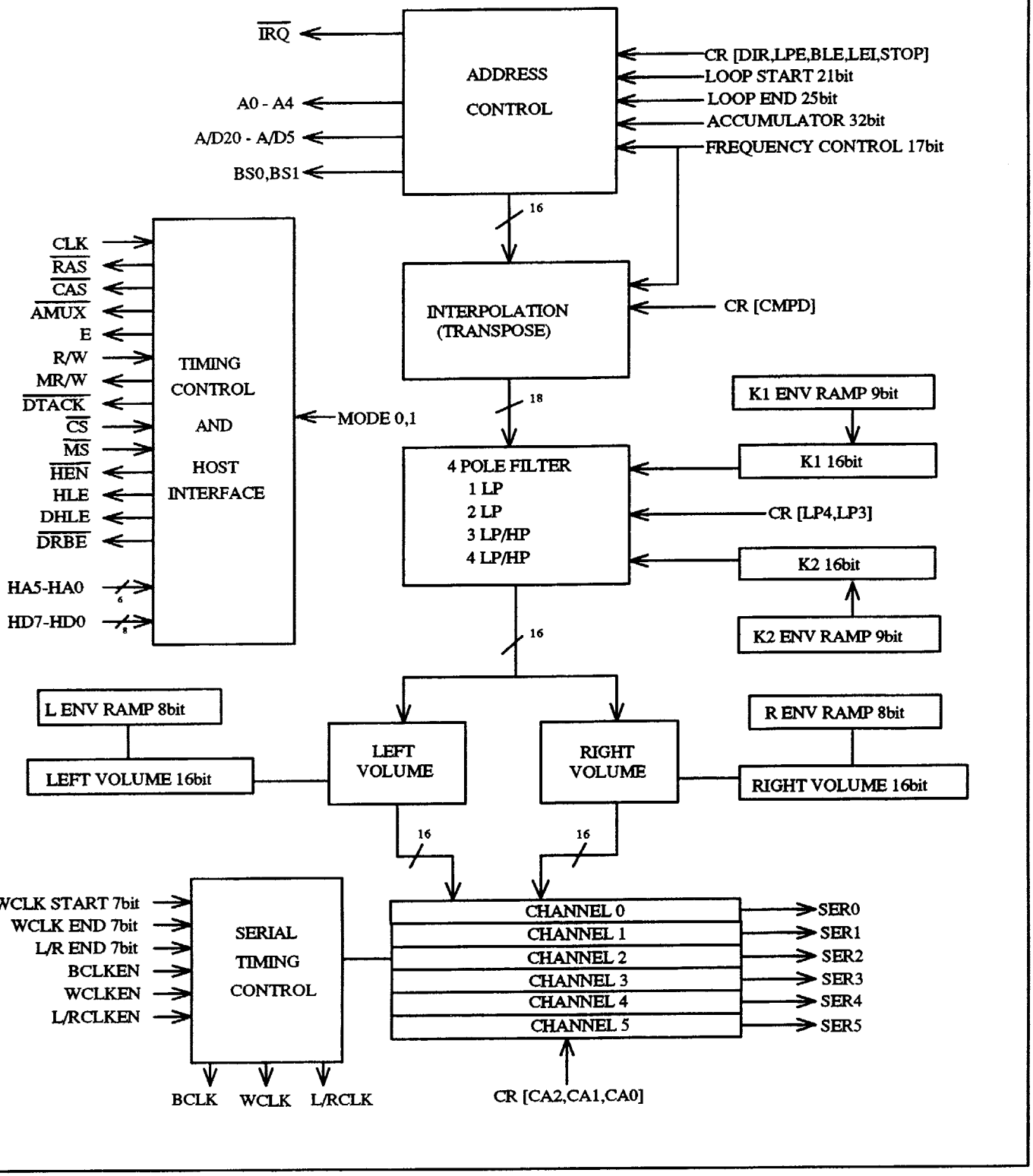
The filtered signal values are multiplied by left and right volume values to provide proper attenuation, and the results are accumulated into one of six serial channels for output. Each voice has registers for defining the volumes and to which output channel the sample is assigned.

Hardware envelope support is provided for volume and filter coefficients. Each voice contains envelope hardware which adds ramp increment values to the volume and filter values once per sample cycle for a programmed number of cycles.

The address generation for each voice consists of a 32-bit Voice Accumulator, a Loop Start Register, a Loop End Register, and a Control Register. The Voice Accumulator contains a 21-bit integer portion and an 11-bit fractional portion. The integer portion of the Voice Accumulator is used to address the external sound memory while the fractional portion is used in the interpolation calculation. The Control Register is used to control interrupts, the various modes of looping, stopping and starting the voice, and a 2-bit bank select to address one of four 2 Megaword banks of memory.

Three global registers are used to set the total number of Active Voices, the Voice Interrupt Vector, and the Page Register. There are sixteen additional registers for setting OTTO modes and testing the channel registers.

OTTO BLOCK DIAGRAM



The CPU accesses all registers through a 6-bit address bus and 8-bit bidirectional data bus. All registers are organized internally as 32-bit wide locations, although not all bits are used in all registers.

2 THE GLOBAL REGISTERS

The Global Registers can be accessed at all times regardless of which voice is being addressed by the page register. These registers control operations which are not voice specific. The following section describes in detail the structure and purpose of each of the registers in the OTTO chip.

NOTE:

The chip follows the Motorola 68000 register address conventions. For example, if the OTTO chip is selected at location 8000_{hex}, then the Page Register is at location 8000_{hex}, and the lowest byte of the Page Register is at location $807B_{hex}$.

2.1 Page Register - PAGE - all pages - loc H78

The page register is used to access the set of fourteen registers which control all aspects of a voice. The Page register appears at location 78_{hex} in all pages. There are a total of sixty-five pages which can be accessed through the page register. The following table describes the register organization for the various pages.

Page # (hex)	Address (hex)	Function
0 - 1F	00 - 50	Voice Specific Control
0 - 1F	58 - 60	Common Control
20 - 3F	00 - 18	Voice Specific Control
20 - 3F	20 - 48	Temp Filter Registers
20 - 3F	50 - 60	Common Control
00 - 3F	68- 78	Global Registers
40	0 - 58	Serial Control Registers

2.2 Voice Interrupt Vector - IRQV - all pages - loc H70

The Voice Interrupt Vector register is used by the microprocessor to determine which voice has caused an interrupt to occur. When a specific voice has its **Interrupt Enable Bit (IEB)** set high in its corresponding control register and the proper events occur to cause an interrupt to be issued, the voice number is placed into this register so that the processor can read the value and determine which voice requires servicing. The IRQB output line of the OTTO chip will go high after the processor reads this register. Bit 7 of this register is a monitor of the IRQB output line and bits 4 through 0 determine the voice interrupt. Conditions sufficient to cause an interrupt will be defined in the Interrupt Control Section.

2.3 Pot A/D Register - PAR - all pages - loc H68

This register contains the 10-bit digital value resulting from the A/D conversion for tracking pots and wheels. The conversion is performed by comparing the input voltage on the POT pin to an internal reference ≅ 2.8V.

A conversion is initiated when the PAR is read. At this time the POT_RES pin is pulled low to discharge the external capacitor. This discharge time lasts for 4*1024*Input Clock Cycle Time. This is 256µsec when the Master clock is 16Mhz.

When POT_RES is released an external R-C charges the POT_IN pin, while the counter is clocked. When the voltage level on the input reaches the internal reference voltage, the value in the counter is loaded into this register for reading by the processor. The counter is clocked at fclk/4. When a conversion is initiated by a read of the PAR , it is set to $3FF_{hex}$ after the read. This is done so that if the external ramp value does not reach the trip point of the comparator the value in the register is maximum.

This type of conversion system is useful for low speed analog voltage conversion which might be used to set the master volume of the system or for voice modulation controllers such as a pitch wheel. Normally these controllers are scanned at a 300Hz rate. To efficiently use the converter, first read the value in the PAR, then wait for a system timer to request an update, then read the new PAR value. From this point on, the CPU can read the PAR for the next conversion value at each system timer request.

At a 16MHz input clock rate a conversion can be performed in 512µsec.

Circuits for use with the A/D are found in the Section 10.4 Pin Description.

3 THE COMMON REGISTERS

3.1 Active Voice Register - ACTV - pages 00 - 1F - loc H58

The Active Voice Register defines how many voices are actually enabled to produce sound. This register uses bits 4 through 0, encoding values 31 through 0. The actual number of active voices is equal to the number in this register plus one. The number of active voices determines the output sample rate of OTTO. Each voice takes 1 microseconds to be processed if OTTO is running at 16MHz. When all 32 voices are active, this corresponds to a 31.2KHz sample rate. A 44.1 KHz sample rate can be achieved by running the OTTO at 16.9 MHz with twenty-four voices enabled. This register initializes to 32 on assertion of RESB. **For proper operation a minimum of five voices must be enabled.**

Sample Rate = Master Clock ÷ (16 × Number of Voices)

3.2 Mode Register - MODE - pages 00 - 1F - loc H60

The Mode Register consists of the following five bits which control the operating modes of the serial data sytem and the dual/slave mode operation of the chip. The serial data channels are clocked and controlled by the BCLK. The number of bit clocks in the sample period is determined by the number of Active Voices. There are four BCLKs per active voice.

LRCLK_EN

The LRCLK_EN bit enables the LRCLK pin as an output when the bit is cleared, allowing the chip to be the master of the serial interface timing. This bit is set high (LRCLK is an input) on assertion of the RESB pin.

WCLK_EN

The WCLK_EN bit enables the WCLK pin as an output when the bit is cleared, allowing the chip to control this signal for serial interface timing. This bit is set high (WCLK is not an output) on assertion of the RESB pin.

OTTO does not use WCLK for any internal serial timing, and therefore this signal is provided for output timing requirements for other devices.

BCLK_EN

The BCLK_EN bit enables the BCLK pin as an output when the bit is cleared, allowing the chip to be the master of the serial interface timing. This bit is set on assertion of the RESB pin.

MODE CONTROL - Master/Slave

These two bits, Mode 1, Mode 0, encode four modes of operation for single and dual OTTO systems as follows.

Dual Mode 1	Master Mode 0	# of OTTO's	Address Function
0	0	Single, Master	Early
0	1	Single, Master	Normal
1	0	Dual, Slave	Normal
1	1	Dual, Master	Normal

If the chip is memory master, its RASB, CASB, AMUXB, and E outputs are enabled to provide the timing for sound memory. In a two-OTTO system, one OTTO should be the master and the other should be the slave. The slave in a two-OTTO systems will synchronize to the E pin of the master so that the two chips will access memory on alternate cycles.

The master clock will output a change of the E signal on the falling edge of the input clock. The slave chip will samples the E signal on the next falling edge of the input clock.

The master chip will always drive the memory timing signals. On RESET, these bits will initialize to MODE1=1, MODE0=0 (Dual OTTO, Slave, Normal Address).

The early address mode is useful for a single OTTO in a ROM only based system where processor access to memory is not required. In early address mode the address change occurs one half cycle early, which is the middle of the previous memory cycle where the HOST access cycle would normally take place, thus allowing additional access time on the ROMS.

3.3 Word Clock Start Register - W_ST - pages 20 - 3F

The W_ST register holds a 7-bit value. This value determines the number of BCLK's after an LRCLK transition before the WCLK output is asserted.

3.4 Word Clock End Register - W_END - pages 20 - 3F - loc H58

The W_END register holds a 7-bit value. This value determines the number of counts after a LRCLK transition before the WCLK output of the chip will be negated. See Section 12 for more information on LR_END, W_ST, and W_END.

3.5 Left/right Clock End Register - LR_END - pages 20 - 3F - loc H60

The LR_END register holds a 7-bit value. This value is the number of BCLK cycles for which the LRCLK output of the chip will be high.

4 THE VOICE SPECIFIC REGISTERS

The following section describes the registers which control a voice in OTTO. The registers for a specific voice are accessed using the A5-A0 address lines. All bits used in the voice specific registers can be read or written by the CPU. Note the abbreviation in parentheses following the register name may be used interchangeably with the complete register name.

There are a total of twenty registers used to control a specific voice. These twenty registers are accessed indirectly via the page register. The control for each voice is spread over two pages. For example Voice 0's registers are found on pages 00 and 20_{hex} and Voice 2's registers are on page 02 and 22_{hex}.

4.1. The Control Register (CR) - pages 00 - 3F - loc H00

The Control Register is a 16-bit register which directs various modes of an OTTO voice. The following is a list of control register bits and their function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BS1	BS0	CMPD	CA2	CA1	CA0	LP4	LP3	IRQ	DIR	IRQE	BLE	LPE	LEI	STP1	STP0

Control Register Bit Locations

4.1.1 Bank Select 1,0 (BS0, BS1)

These bank select bits are output on the BS[1:0] pins at the same time as address for a memory cycle. They can be used to select between four 2Meg Samples banks of RAM in an 8Meg Sample system. They can also be used as an external indication of the state of the internal voice counter.

4.1.2 Compressed Mode (CMPD)

This bit is used to select between linear data mode and compressed data mode. When this bit is set, the data accessed from sound memory for this oscillator is stored in compressed format (see section 5.2 for more information on compressed data mode.

4.1.3 Channel Assign (CA2, CA1, CA0)

The Channel Assign information is a 3-bit code used to specify an output channel for the current voice. There are six serial output channels: 0 to 5. When more than one voice is assigned to a channel, the volume of each voice may need to be adjusted to avoid overflow conditions in a channel.

4.1.4 Low Pass Filter Mode (LP4, LP3)

The Filter Configuration bits define the four possible modes of the digital filter. The two bits used are referred to as LP4 and LP3, which are lowpass filter 4 and lowpass filter 3, respectively. In the digital filter, filters 1 and 2 are always low pass and use coefficient K1.

The following chart indicates these configurations.

Filter Configuration and Coefficient Assignment Table

LP4	LP3	Filter 4 Mode	Filter 4 Coefficient	Filter 3 Mode	Filter 3 Coefficient
0	0	HighPass	K2	HighPass	K2
0	1	HighPass	K2	LowPass	K1
1	0	LowPass	K2	LowPass	K2
1	1	LowPass	K2	LowPass	K1

The above chart shows the mode (low or high pass) of the filter and the coefficient value used in the filter computation.

4.1.4 IRQ

A status flag showing that this voice has requested service through the Voice Interrupt Vector or has an interrupt request pending and is waiting for the Voice Interrupt Vector to be cleared of the current voice.

4.1.5 Direction (DIR)

This bit indicates the direction the sample is being scanned by the address ALU. A zero indicates the forward (incrementing) through memory, a one indicates the decrementing case. If the bidirectional looping mode has been selected the address ALU will automatically toggle this bit when the address reaches either the Loop Start or Loop End positions.

4.1.6 Interrupt Enable (IRQE)
This bit enables the Interrupt for the voice if IRQE=1.

4.1.7 Loop Control (BLE, LPE)
These two bits encode four different looping states as follows.

BLE	LPE	FUNCTION
0	0	no looping
0	1	uni-directional looping
1	0	trans wave looping
1	1	bi-directional looping

Looping is enabled if either LPE or BLE are 1. Looping refers to restoring the address accumulator to the Loop Start position when the address accumulator exceeds the value in the Loop End register. If LPE and BLE are zero then the accumulator will stop when it reaches Loop End. The role of the Start and Stop positions is reversed if the DIR bit is a one. An additional looping mode is available, trans-wave looping mode. In this mode the address accumulator jumps to loop start (adding the fractional portion) when loop end is reached. The BLE bit is cleared and the LEI (Loop End Ignore) bit is set. This mode is useful to create waveforms that have loops which appear to evolve and modulate so that the loop does not sound stagnant. For more information about Phase Accunulating Counters see Section 11.

4.1.8 Loop End Ignore (LEI)
LEI is the loop end ignore bit. It has the function of causing the chip to ignore the result of the check for loop end. This is necessary for the new trans-wave mode where the waveform position jumps around through memory. When loop end is detected in transwave mode, the chip jumps to a new loop start (which may be greater than loop end). The chip is set to "no looping mode" with the loop end ignore bit set so the accumulator does not stop. The accumulator will run until the host comes in and updates the loop end register and sets up the proper looping mode.

4.1.9 STOP1
This bit is used by the processor to stop the address ALU from modifying any bits in a voice during its normal processing. For example, if this bit is set then the newly calculated address for the next sample will not be stored into the address accumulator or the direction bit will not be changed. This feature allows the microprocessor to change the contents of either the control register or accumulator.

Note on Running Voices:
When a voice is running care must be taken when changing information that controls a voice. There is a three voice pipeline within the OTTO chip that may over write data written by the CPU. The DIR, STOP0, LEI and IRQ bits, the ACCUMULATOR, and the Filter Temp Registers, the VOLUME, and the Filter Coefficients K1 and K2 are changed by OTTO during normal operation. If the CPU modifies these bits or registers it

is recommended that they are written twice, at least three microseconds apart to avoid collision with the internal pipeline write.

4.1.10 STOP0

This bit performs the same function as the STOP1 bit. The difference is that this bit can be set by the address ALU. This bit is set when Looping is disabled and the accumulator reaches the Loop Stop position. Note that both STOP1 and STOP0 must equal zero for the voice to run.

4.2 The Start Registers (START) - pages 20 - 3F - loc H08

The Start Register, also called the Loop Start Register, is a 21-bit value. The Loop Start position, as its name implies, is used to define where in the sample memory the accumulator will jump to when it reaches the Loop End position. Note that the Loop Start register has a 21-bit integer portion and no fractional portion.

4.3 The End Registers (END) - pages 20 - 3F - loc H10

The End Register, also called the Loop End Register is a 25-bit register used to mark the end of a loop in the sample memory. Note that the Start and End Registers reverse their roles if the Direction bit is a one. The End register contains the same 21-bit integer portion as start but is has a 4-bit fractional portion for finer control of loop points.

4.4 Accumulator (ACCUM) - pages 20 - 3F - loc H18

The Accumulator is a 32-bit register. The Accumulator is comprised of an integer portion and a fractional portion. The integer part is 21 bits which is the actual information used to fetch the sample data from memory. The 11-bit fractional part is needed to obtain proper frequency resolution and also for the interpolation calculation (discussed in the Signal Processing section).

The Accumulator is also used as the waveform start position. This is not to be confused with the use of the Loop Start register. The initial Accumulator value is the beginning of the waveform while the Loop Start position defines the beginning of the sustain part of the waveform.

Note that a write to this register by the CPU may be overwritten when OTTO increments the accumulator for an active (not stopped) voice.

4.5 The Frequency Control Register (FC) - pages 00 - 1F - loc H08

The Frequency Control Register is used to define the rate at which the address ALU will step through the sample memory. The register is a 17-bit word, that is divided into a 6-bit integer portion and a 11-bit fractional portion.

4.6 Left Volume (LVOL) - pages 00 - 1F - loc H10

The Left Volume Register is a 16-bit register used to define the effective amplitude of the left channel of the signal. It contains a 4-bit exponent in the MSBs and an 8-bit

mantissa in the next lower bits. These 12-bits are used for the panning calculation. The remaining four LSBs are used for fine control of the ramp increment for hardware envelopes.

When the Control Register STOP1 or STOP0 bit is set, the LVOL value is ignored and the volume is set to zero.

Note that a write to this register by the CPU may be overwritten when hardware envelope system increments the filter value of an active (not stopped) voice.

4.7 Left Volume Ramp (LVRAMP) - pages 00 - 1F - loc H18

The Left Volume Ramp Register is used by the envelope hardware to ramp (increment) the value in LVOL. It is an 16-bit register containing an 8-bit ramp amount in the MSBs; the eight LSBs are not implemented. The use of this register will be discussed in the explanation of the Hardware Envelope Algorithm. See Section 11.5.

4.8 Right Volume (RVOL) - pages 00 - 1F - loc H20

This register is used to define the effective amplitude of the right channel of the sampled signal. It's contents match those of LVOL. Together with LVOL it allows amplitude manipulation and stereo panning.

When the Control Register STOP1 or STOP0 bit is set, the RVOL value is ignored and the volume is set to zero.

4.9 Right Volume Ramp (RVRAMP) - pages 00 - 1F - loc H28

The Right Volume Ramp Register is used by the envelope hardware to ramp the value in RVOL. It is an 16-bit register containing an 8-bit ramp amount in the MSBs; the eight LSBs are not implemented. The use of this register will be discussed in the explanation of the Hardware Envelope Algorithm. See Section 11.5.

4.10 Envelope Counter (ECOUNT) - pages 00 - 1F - loc H30

The Envelope Count Register is a nine bit counter used for setting the duration of a ramp. The counter is set to a starting value and decrements once per sample period. When the counter reaches zero, the envelope calculation is inhibited from updating the volume and filter coefficients for that voice. The use of this register will be discussed further in the explanation of the Hardware Envelope Algorithm.

When the Envelope Counter is zero, the values in the Filter Coefficients and the Volume Registers can be changed and will not be overwritten by the chip pipeline. This feature is active only when the Envelope Counter is zero.

If the CPU writes a value other than zero to the ECOUNT Register, it may be overwritten. Therefore, the CPU should first write a zero to this register followed by a write of the new value separated by one sample period. The chip pipeline can also be defeated by writing the new value twice with a 3 µsec delay between writes.

4.11 Filter Coefficient 2 (K2) - pages 00 - 1F - loc H38

The Filter Coefficient 2 Register is used to determine the 3dB point of filters three and four of the digital filter. It is a 16-bit register, of which the 12 MSBs are used in the filter calculation. The four LSBs allow for fine control of ramp increments for envelopes. The use of this register will be discussed in the explanation of the Digital Filter. See Filter Coefficient Assignment Table in Section 4.1.4 for information on how K2 is applied to filters 3 and 4.

Note that a write to this register by the CPU may be overwritten when hardware envelope system increments the filter value of an active (not stopped) voice (see Envelope Counter Description for exception).

4.12 Filter Coefficient 2 Ramp (K2RAMP) - pages 00 - 1F - loc H40

The Filter Coefficient 2 Ramp Register is used by the envelope hardware to ramp the value in K2. It is 16-bit register, of which the eight MSBs are the ramp amount. The LSB is a control which when set puts the envelope into a slower mode with the increment being added every eight sample periods rather than once every sample period. The use of this register will be discussed in the explanation of the Hardware Envelope Algorithm.

4.13 Filter Coefficient 1 - pages 00 - 1F - loc H48

The Filter Coefficient 1 Register is used to determine the 3dB point of filters one, two and/or three of the digital filter. It is a 16-bit register, of which the twelve MSBs are used in the filter calculation. The four LSBs allow for fine control of ramp increments for envelopes. The use of this register will be discussed in the explanation of the Digital Filter. See Filter Coefficient Assignment Table in Section 4.1.4 for information on how K2 is applied to filters 2 and 3.

Note that a write to this register by the CPU may be overwritten when hardware envelope system increments the filter value of an active (not stopped) voice (see Envelope Counter Description for exception).

4.14 Filter Coefficient 1 Ramp (K1RAMP) - pages 00 - 1F - loc H50

The Filter Coefficient 1 Ramp Register is used by the envelope hardware to ramp the value in K1. It is 16-bit register, of which the eight MSBs are the ramp amount. The LSB is a control bit which when set puts the envelope into a slower mode with the increment being added every eight sample periods rather than once every sample period. The use of this register will be discussed in the explanation of the Hardware Envelope Algorithm.

5 THE FILTER STORAGE REGISTERS

The Filter Storage Registers are used as temporary storage locations for the real time digital filters in each voice. Each digital filter requires six 18-bit registers to complete is calculations. These six registers are addressable by the processor mainly for testing purposes and initialization, but there may be some yet to be determined audio benefits achieved by some real time processor intervention.

These registers are continuously updated even when the voice is stopped. Since the addresses bus to the sound memory is not enabled when a voice is stopped, the data that flows to the filter section may be invalid. This is acceptable since the volume is forced to zero when a voice is stopped. A problem can occur however, if a voice is activated before the four filter temp registers clear out the invalid data. A procedure for avoiding this problem will presented in the Voice Set Up section. See Section 11.4

5.1 Filter Temp Reg O4(n-1) - pages 20 - 3F - loc H20

This 18-bit register contains the output of final stage of the digital filter. This register contains the data presented to the volume multiplication and channel accumulation hardware.

5.2 Filter Temp Reg O3(n-1) - pages 20 - 3F - loc H28

This 18-bit register contains the output of the third stage of the digital filter. The output of this stage is the input to the fourth stage and the data is pushed into Pole 3(n-2) on the next cycle.

5.3 Filter Temp Reg O3(n-2) - pages 20 - 3F - loc H30

This 18-bit register stores the output of the third stage of the digital filter from the previous sample period. This information is needed to process the high pass filter mode of filter pole 4.

5.4 Filter Temp Reg O2(n-1) - pages 20 - 3F - loc H38

This 18-bit register contains the output of the second stage of the digital filter. The output of this stage is the input to the third stage and the data is pushed into Pole 2(n-2) on the next cycle.

5.5 Filter Temp Reg O2(n-2) - pages 20 - 3F - loc H40

This 18-bit register stores the output of the second stage of the digital filter from the previous sample period. This information is needed to process the high pass filter mode of filter pole 3.

5.6 Filter Temp Reg O1(n-1) - pages 20 - 3F - loc H48

This 18-bit register contains the output of the first stage of the digital filter. The output of this stage is the input to the second stage.

6 THE CHANNEL REGISTERS - page 40_{hex}

Page 64 is used to address twelve output channel registers. The channel registers are used to accumulate the information from the voices assigned to that particular channel during a sample period. These registers are global to this address space and are accessed when the MSB of the page register is a 1. All the Channel register are 23 bits right justified. The upper three bits are three overflow guard bits . The lower 20 data bits are transferred to the serial output register. If an overflow or underflow condition is present at the time of transfer to the output, the data is saturated to the appropriate rail so that data "wrapping" does not occur.

The test mode of the channel registers can be useful in debugging the output circuitry on the PCB. Set the test bit in the PAGE register and the CPU can write directly to the

Channel Registers. The data written to the Channel registers is shifted out through the corresponding serial output.

6.1 Channel 0 Left/Right (CH0L/CH0R)- loc H00,H08

These 23-bit registers contain the accumulation of the result of the left and right volume multiplication for any voice assigned to Channel 0. The registers are connected to serial port 0. They can be accessed only for testing these output sections. Therefore they can be written, but can not be read.

6.2 Channel 1 Left/Right (CH1L/CH1R)- loc H10,H18

These registers have the same function as CH0L/CH0R. The registers are connected to serial port 1 and can be access for testing in the same way as CH0L/CH0R.

6.3 Channel 2 Left/Right (CH2L/CH2R)- loc H20,H28

Same as CH0L/CH0R, but connected to serial port 2.

6.4 Channel 3 Left/Right (CH3L/CH3R)- loc H30,H38

Same as CH0L/CH0R, but connected to serial port 3.

6.5 Channel 4 Left/Right (CH4L/CH4R)- loc H40,H48

Same as CH0L/CH0R, but connected to serial port 4.

6.6 Channel 5 Left/Right (CH5L/CH5R)- loc H50,H58

Same as CH0L/CH0R, but connected to serial port 5.

7 REGISTER MAP

Pages 0 to 20_{hex}

REG	Symbol	Description	Bits	Justification
0	CR	Control Register	16	15:0
1	FC	Frequency Control	17	16:0
2	LVOL	Left Volume	16	15:0
3	LVRAMP	Left Volume Ramp	8	15:8
4	RVOL	Right Volume	16	15:0
5	RVRAMP	Right Volume Ramp	8	15:8
6	ECOUNT	Envelope Counter	9	8:0
7	K2	Filter Coeff #2	16	15:0
8	K2RAMP	Filter Cutoff #2 ramp	9	15:8,0
9	K1	Filter Coeff #1	16	15:0
10	K1RAMP	Filter Cutoff #1 ramp	9	15:8,0
11	ACTV	Active voices	5	4:0
12	MODE	Global Mode	5	4:0
13	POT	Pot A/D Register	10	9:0
14	IRQV	Interrupt voice vector	5	4:0
15	PAGE	Page select Register	7	6:0

Pages 20_{hex} to $3F_{hex}$

REG	Symbol	Description	Bits	Justification
0	CR	Control Register	16	15:0
1	START	Loop Start	21	31:11
2	END	Loop End	25	31:7
3	ACCUM	Address Accumulator	32	31:0
4	O4(n-1)	Filter#4 Temp	18	17:0
5	O3(n-1)	Filter#3 Temp	18	17:0
6	O3(n-1)	Filter#3 Temp	18	17:0
7	O2(n-1)	Filter#2 Temp	18	17:0
8	O2(n-1)	Filter#2 Temp	18	17:0
9	O1(n-1)	Filter#1 Temp	18	17:0
10	W_ST	Word Clock Start	7	6:0
11	W_END	Word Clock End	7	6:0
12	LR_END	Left/Right Clock End	7	6:0
13	POT	Pot A/D Register	10	9:0
14	IRQV	Interrupt voice vector	5	4:0
15	PAGE	Page select Register	7	6:0

Page 40_{hex}

Registers 0 to 11 are write-only for testing purposes.

REG	Symbol	Description	Bits	Justification
0	CH0L	Channel 0 Left	23	22:0
1	CH0R	Channel 0 Right	23	22:0
2	CH1L	Channel 1 Left	23	22:0
3	CH1R	Channel 1 Right	23	22:0
4	CH2L	Channel 2 Left	23	22:0
5	CH2R	Channel 2 Right	23	22:0
6	CH3L	Channel 3 Left	23	22:0
7	CH3R	Channel 3 Right	23	22:0
8	CH4L	Channel 4 Left	23	22:0
9	CH4R	Channel 4 Right	23	22:0
10	CH5L	Channel 5 Left	23	22:0
11	CH5R	Channel 5 Right	23	22:0

Global Mode Register bit definition

Bit	Name	Function
0	LRCLK_EN	Enable LRCLK as output - low active.
1	WCLK_EN	Enable WCLK as output - low active.
2	BCLK_EN	Enable BCLK as output - low active.
3	MODE0	Set chip as memory bus master.
4	MODE1	The chip is in a two OTTO system.

Oscillator Control Register Bit Definition - CR

Bit	Name	Function
0	STP0	Oscillator Stop Bit.
1	STP1	Processor Oscillator Stop Bit.
2	LEI	Loop End Ignore.
3	LPE	Loop Enable.
4	BLE	Bidirectional Loop Enable.
5	IRQE	Interrupt Enable
6	DIR	Direction
7	IRQ	Interrupt
8	LP3	Low pass pole 3.
9	LP4	Low pass pole 4.
10	CA0	Channel Assign 0.
11	CA1	Channel Assign 1.
12	CA2	Channel Assign 2.
13	CMPD	Compressed Sample Data.
14	BS0	Bank Select 0.
15	BS1	Bank Select 1.

OTTO REGISTER MAP

PAGE = 00 - 1F

	LOC	REGISTER NAME	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			CONTROL REGISTER FUNTIONS																BANK SELECT		COMPRESSED DATA	OUTPUT ASSIGN			FILTER MODE		IRQ STATUS	DIRECTION (1=FORWARD)	IRQ ENABLE	LOOP CONTROL		CPU STOP		OSC STOP
	00	CONTROL REGISTER	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BS1	BS0	CMPD	CA2	CA1	CA0	LP4	LP3	IRQ	DIR	IRQE	BLE	LPE	LEI	STP1	STP0
	08	FREQUENCY	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	I5	I4	I3	I2	I1	I0	FI0	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
	10	LEFT VOLUME	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	EX3	EX2	EX1	EX0	M7	M6	M5	M4	M3	M2	M1	M0	VF3	VF2	VF1	VF0
	18	LEFT VOLUME RAMP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	RM2	RM1	RM0	RF3	RF2	RF1	RF0	X	X	X	X	X	X	X	X
	20	RIGHT VOLUME	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	EX3	EX2	EX1	EX0	M7	M6	M5	M4	M3	M2	M1	M0	VF3	VF2	VF1	VF0
	28	RIGHT VOLUME RAMP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	RM2	RM1	RM0	RF3	RF2	RF1	RF0	X	X	X	X	X	X	X	X
	30	ENVELOPE COUNTER	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
	38	FILT 2 CUTOFF FREQ	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	FC11	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FCF3	FCF2	FCF1	FCF0
	40	FILT 2 CUTOFF RAMP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	RM2	RM1	RM0	RF3	RF2	RF1	RF0	X	X	X	X	X	X	X	SLOW
	48	FILT 1 CUTOFF FREQ	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	FC11	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FCF3	FCF2	FCF1	FCF0
	50	FILT 1 CUTOFF RAMP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	RM2	RM1	RM0	RF3	RF2	RF1	RF0	X	X	X	X	X	X	X	SLOW
COMMON	58	NUMBER OF VOICES	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	AV4	AV3	AV2	AV1	AV0
COMMON	60	GLOBAL MODES	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DUAL	MSTR	BCLK	WCLK	IRCLK
GLOBAL	68	POTA/D REG	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
GLOBAL	70	VOICE INTRPT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	I	X	X	V4	V3	V2	V1	V0
GLOBAL	78	PAGE SELECT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TEST	PS5	PS4	PS3	PS2	PS1	PS0

LOW ACTIVE

OTTO REGISTER MAP

PAGE = 20 - 3F

LOC	REGISTER NAME	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		CONTROL REGISTER FUNTIONS															BANK SELECT			COMPRESSED DATA	OUTPUT ASSIGN		FILTER MODE		IRQ STATUS	DIRECTION (1=FORWARD)	IRQ ENABLE	LOOP CONTROL			CPU STOP	OSC STOP
00	CONTROL REGISTER	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BS1	BS0	CMPD	CA2	CA1	CA0	LP4	LP3	IRQ	DIR	IRQE	BLE	LPE	LEI	STP1	STP0
08	LOOP START	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	F10	F9	F8	F7	X	X	X	X	X	X	X
10	LOOP END	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	F10	F9	F8	F7	X	X	X	X	X	X	X
18	ACCUMULATOR	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
20	FILTER4 TMP O4 (N-1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	SIGN	HD14	HD13	HD12	HD11	HD10	HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	HDF0
28	FILTER3 TMP O3 (N-1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	SIGN	HD14	HD13	HD12	HD11	HD10	HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	HDF0
30	FILTER3 TMP O3 (N-2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	SIGN	HD14	HD13	HD12	HD11	HD10	HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	HDF0
38	FILTER2 TMP O2 (N-1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	SIGN	HD14	HD13	HD12	HD11	HD10	HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	HDF0
40	FILTER2 TMP O2 (N-2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	SIGN	HD14	HD13	HD12	HD11	HD10	HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	HDF0
48	FILTER1 TMP O1 (N-1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SIGN	SIGN	HD14	HD13	HD12	HD11	HD10	HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	HDF0
50	WORD CLK STRT * BLOCK AFTER LRCLK	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BC6	BC5	BC4	BC3	BC2	BC1	BC0
58	WORD CLK END * BLOCK AFTER LRCLK	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BC6	BC5	BC4	BC3	BC2	BC1	BC0
60	L/R CLOCK END * BLOCK WIDE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BC6	BC5	BC4	BC3	BC2	BC1	BC0
68	POT A/D REG	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P7	P6	P5	P4	P3	P2	P1	P0
70	VOICE INTRPT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	I	X	X	V4	V3	V2	V1	V0
78	PAGE SELECT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TEST	RS5	RS4	RS3	RS2	RS1	RS0

COMMON

GLOBAL

OTTO REGISTER MAP

PAGE = 40 write only

LOC	REGISTER NAME	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CHANNEL 0 LEFT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
08	CHANNEL 0 RIGHT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
10	CHANNEL 1 LEFT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
18	CHANNEL 1 RIGHT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
20	CHANNEL 2 LEFT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
28	CHANNEL 2 RIGHT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
30	CHANNEL 3 LEFT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
38	CHANNEL 3 RIGHT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
40	CHANNEL 4 LEFT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
48	CHANNEL 4 RIGHT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
50	CHANNEL 5 LEFT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
58	CHANNEL 5 RIGHT	X	X	X	X	X	X	X	X	X	G	G	G	SD19	SD18	SD17	SD16	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
60	EMPTY	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
68	POTA/D REG	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P4	P3	P2	P1	P0
70	VOICE INTRPT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	V4	V3	V2	V1	V0
78	PAGE SELECT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TEST	RS5	RS4	RS3	RS2	RS1	RS0

GLOBAL

8 VOICE SETUP

The proper procedure for setting up a voice is as follows:

1. Set STOP1 bit to 1
2. Set ECOUNT to 0
3 Set LP4 and LP3 to LowPass filter mode (LP4=LP3=1)
4. Set ACCUM to waveform start address
5. Set K1 and K2 to FFF_{hex} - allows any data in the filters to clear. This may take up to four sample periods.
6. Set FC to desired transposition value
7. Set START to Loop Start Address
8. Set END to Loop End Address
9. Set LVRAMP and RVRAMP increment values
10. Set K1RAMP and K2RAMP increment values
11. Set LP4, LP3 to disired filter mode
12. Set K1 and K2 to the desired filter cutoff values
13. Set LVOL and RVOL to desired values
14. Set ECOUNT to desired value
15. Set STOP1 and STOP0 to 0

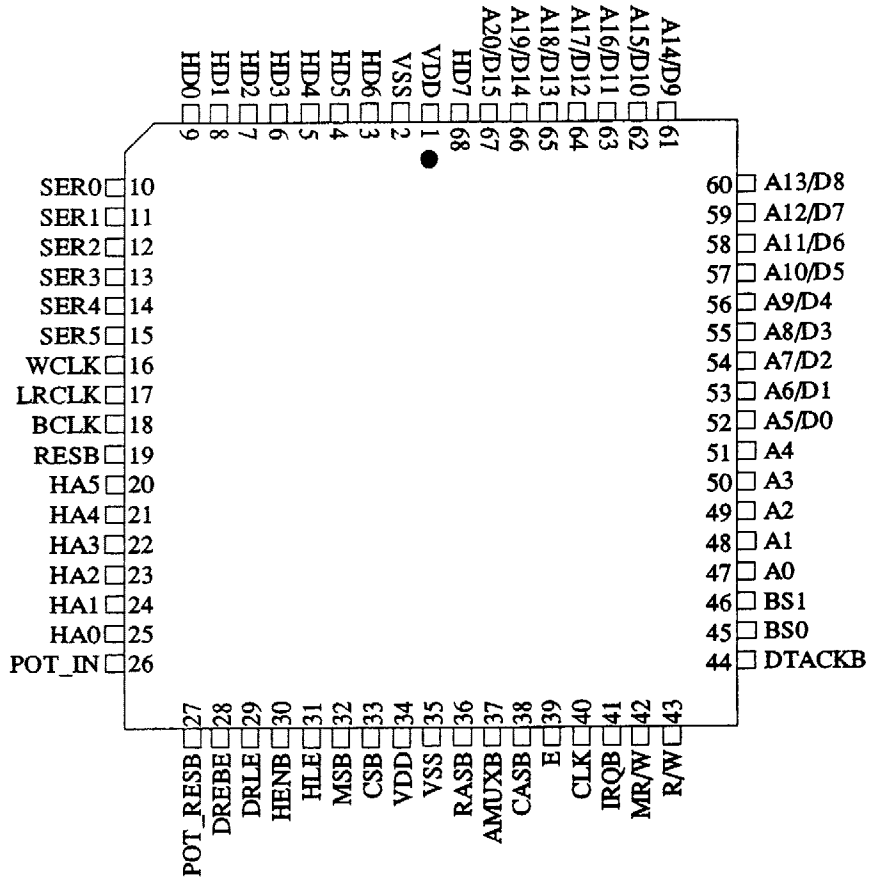
Note on Running Voices:

When a voice is running care must be taken when changing information that controls a voice. There is a three voice pipeline within the OTTO chip that may over write data written by the CPU. The DIR, STOP0, LEI and IRQ bits, the ACCUMULATOR, and the Filter Temp Registers, the VOLUME, and the Filter Coefficients K1 and K2 are changed by OTTO during normal operation. If the CPU modifies these bits or registers it is recommended that they are written twice, at least three microseconds apart to avoid collision with the internal pipeline write.

9 PINOUT

The chip is a 68 pin PLCC.

1	VDD	18	BCLK	35	VSS	52	A5/D0
2	VSS	19	RESB	36	RASB	53	A6/D1
3	HD6	20	HA5	37	AMUXB	54	A7/D2
4	HD5	21	HA4	38	CASB	55	A8/D3
5	HD4	22	HA3	39	E	56	A9/D4
6	HD3	23	HA2	40	CLK	57	A10/D5
7	HD2	24	HA1	41	IRQB	58	A11/D6
8	HD1	25	HA0	42	MR/W	59	A12/D7
9	HD0	26	POT_IN	43	R/W	60	A13/D8
10	SER0	27	POT_RES	44	DTACKB	61	A14/D9
11	SER1	28	DRBEB	45	BS0	62	A15/D10
12	SER2	29	DRLE	46	BS1	63	A16/D11
13	SER3	30	HENB	47	A0	64	A17/D12
14	SER4	31	HLE	48	A1	65	A18/D13
15	SER5	32	MSB	49	A2	66	A19/D14
16	WCLK	33	CSB	50	A3	67	A20/D15
17	LRCLK	34	VDD	51	A4	68	HD7



9.1 Memory interface

Pin	Description	# of pins
A[4:0]	low address	5
A/D[20:5]	multiplexed address/data	16
BS[1:0]	bank select	2
RASB	row address strobe	1
CASB	column address strobe	1
AMUXB	address mux control	1
MR/W	memory read/write	1

9.2 Host interface

Pin	Description	# of pins
R/W	read/write	1
MSB	memory select	1
CSB	chip select	1
DTACKB	data transfer acknowledge	1
HA[5:0]	host address	6

HD[7:0]	host data	8
IRQB	interrupt request	1
HENB	Host Address Buffer Enable	1
HLE	Host address/data Latch Enable	1
DRLE	Data Read Latch Enable	1
DRBEB	Data Read Buffer Enable	1

9.3 Miscellaneous

SER[5:0]	Serial data	6
BCLK	Bit Clock	1
WCLK	Word Clock	1
LRCLK	Left/Right Clock	1
E	Enable Clock.	1
CLK	Clock	1
RESET	Reset	1
POT_IN	Pots and wheels comparator input	1
POT_RES	Pots and wheels reset output	1
SUPPLIES	2 vdd's 2 vss's	4

10 THE PIN DESCRIPTIONS

The following section describes the function of each of the pins of OTTO.

CLK

The CLK pin is the input clock for OTTO. The clock can be any frequency from 8 Mhz to 16.9 Mhz. The clock input should be as close to 50-50 duty cycle as possible, since the chip times events on both input clock edges.

RESB

The RESB pin is the reset input to OTTO. It initializes the operating mode of the chip and also the state of the internal clocks and oscillator counter for test purposes.

10.1 MEMORY INTERFACE

A0-A4

These five output lines form the low address the external sound memory. These pins will output the voice address at the falling edge of the E for the MASTER OTTO and the rising edge of E for the SLAVE OTTO. The address will remain valid during the appropriate phase of E. The pins will go to a high impedance state during the opposite phase of E. These pins are high impedance for master DUAL OTTO mode during a stopped oscillator to avoid contention with DMA address information. In early address mode, the address is asserted at the fall of CASB during the previous memory cycle.

A5/D0 - A20/D15

These sixteen lines are bidirectional. They supply the high address to the memory and perform the data transfers from the memory to OTTO. The function of this bus depends on the state of the E clock. When the E clock is low these lines are first used to output the address for the sound memory access. The lines A0 through A4 together with A5 through A20 form the entire 21-bit address generated by OTTO. The addresses A4 through A19 will turn on one clock phase after E goes low. The address will remain valid until the fall of CASB at which time the bus will go to the input mode to accept the data from the memory (D0 through D15).

For a SLAVE OTTO this activity takes place during E high. In early address mode address is asserted at the fall of CASB during the previous memory cycle.

In Master DUAL OTTO mode these pins will be in a high impedance state during a stopped voice address cycle.

BS[1:0]

When the E clock is low these pins follow the BS1,0 bits of the voice specific control register. It can be used to select between four 2Mword banks of sound memory. Since the state of this bit is voice dependent, it can also be used as an external indication as to the state of the voice counter. A SLAVE OTTO will assert its Bank Select pins during E high.

In Early Address Mode this siganl is asserted at the fall of CASB of E high time.

In Master DUAL OTTO mode these pins will be in a high impedance state during a stopped voice address cycle

MR/W

The MR/W pin is the Write Enable signal to memory. Writing of memory takes place on host writes to memory, which is executed under OTTO's control. Memory writes can take place during E high in a single OTTO system or during E low of a stopped oscillator in a dual OTTO system. See the description of the Host interface for more information on HOST to memory DMA.

RASB

The RASB pin is an output pin which generates a clock used to strobe the row address information into dynamic rams. This clock falls one cycle after an E clock transition. The RAS clock is high for two clock cycle and low for two clock cycles. The memory clocks are free running since the OTTO chip has control of the MR/W line which is the Write Enable to the memory.

CASB

The CASB pin is an output pin which generates a clock used to strobe the column address information into dynamic rams. This clock occurs in the same manner as RASB. The CASB clock is high for two clock cycles and low for two clock cycles. Its falling edge will occur 1 clock cycle after the falling edge of RAS.

AMUXB

The AMUXB pin is an output pin which generates a clock used to multiplex the row addresses and column addresses to the dynamic ram. The AMUXB line is generated whenever RASB and CASB occurs. This clock is high for two clock cycles and low for two clock cycles. Its falling occurs exactly one half cycle between the RASB falling edge and the CASB falling edge.

E

The E clock is an output used to indicate the current state of the OTTO chip. OTTO uses a shared bus structure. In a single-OTTO system, when the E signal is low OTTO accesses memory for sound generation and when E is high OTTO and the sound memory are available for access by the processor. In a dual-OTTO system, the master OTTO will access sound memory during E low for both sample fetching and DMA. The slave OTTO will fetch samples during E clock high time. The E clock is high for four clock cycles and low for four clock cycles.

10.2 CONTROL

R/W

The R/W pin is an input that controls the direction of the data transfer between OTTO and the processor. When R/W is low the processor is writing data into OTTO. The R/W line is strobed at the rising edge of the E clock and if the CSB line is low OTTO will respond to the read/write request.

CSB

The CSB (Chip Select) pin is an input used to select OTTO for a read or write operation. The CSB line is strobed at the rising edge of the E clock and if the CSB line is low OTTO will perform the operation requested by the R/W signal and generate a DTACKB signal.

The HD[7:0] lines will remain valid for one half E cycle beyond the fall of the E clock. Therefore CSB and MSB should not be extended beyond this time.

MSB

The MSB (Memory Select) pin is an input used to assist in the processor access of shared dynamic memory. The MSB line is strobed at the rising edge of the E clock. When OTTO detects MSB is low it will control the execution of the processor to memory cycle based on such factors as a single or dual OTTO system and the occurrence of stopped voices. See the description of the host interface for more details.

The HD[7:0] lines will remain valid for one half E cycle beyond the fall of the E clock. Therefore CSB and MSB should not be extended beyond this time.

DTACKB

The DTACKB pin is an open drain output used to synchronize the transfer of data between a microprocessor and OTTO or memory. The DTACKB signal will go low to

acknowledge the completion of the data transfer. The DTACKB pin goes low two clock cycles after an edge of the E clock and will release when CSB and MSB go high.

Note that the Dtack line is asserted before the HD[7:0] siganls become valid. This was done because the 68000 will latch data one cycle after the DTACK line is recognized. When using a very high speed CPU be sure that the DTACK to data valid time is acceptable.

The HD[7:0] lines will remain valid for one half E cycle beyond the fall of the E clock. Therefore CSB and MSB should not be extended beyond this time.

IRQB

The IRQB pin is an open drain output used to signal the processor that a special case has occurred that requires servicing. The line will go low when the interrupt is required by a particular voice. When the processor reads the Voice Vector register the line will then be released.

HA[5:0]

These six pins are the processors address to OTTO for accessing OTTO chip registers. The address should be valid before the assertion of CSB.

HD[7:0]

These eight pins are the processor data interface to OTTO. Data should be valid at the time CSB is asserted. See the description of the host interface for additional information.

The HD[7:0] lines will remain valid for 1/2 E cycle beyond the fall of the E clock. Therefore CSB and MSB should not be extended beyond this time.

HENB

HENB is the HOST Address Enable pin used to control external tristate buffers for driving host address onto the sound memory address bus. HENB is a low active signal. This pin is only used in a dual OTTO system. In a single OTTO system the enable for the address latch is control by the E clock. (see Host Block Diagrams)

HLE

HLE is the Host Latch Enable signal. It is a high active signal used to trigger a register for latching processor address for host to memory access. It is also used to latch the high byte of a 16-bit data word during a processor write of memory. This signal is used to gate the data from the CPU into a latch. (see Host Block Diagrams)

DRLE

Data Read Latch Enable is a high active signal used to gate the high byte of a 16-bit data word during a processor read of memory. This is required because of the asynchronous nature of the host and OTTO timing. This signal is intended to control an external transparent latch (74ls373).

In slave mode this pin reflects the state of the internally generated M/S (E) clock. This output clock should be 180° out of phase form the E clock of the Master OTTO. This feature aids in the debugging process.

DRBEB

Data Read Buffer Enable is a low active signal used to control the output enable of the data read latch. It is active during a processor read of memory, and remains active until MSB is negated signaling the end of the cycle.

10.3 SERIAL OUTPUT PORTS

BCLK

This is the bit clock for transfers on the serial port. It is a free-running divide by four of the CLK input. See the description of the Serial Interface for additional information.

WCLK

This is the word clock for transfers on the serial port. A low going transition on this clock signals the end of a word transfer. See the description of the Serial Interface for additional information.

LRCLK

his is the left/right clock for transferring stereo information. It signifies left when in the high state and right when in the low state. See the description of the Serial Interface for additional information.

NOTE: The LRCLK pin must be low when this signal is enabled in the Global Modes Control Register. If the this pin is high when enabled the LRCLK output will not function properly. A 2.7KΩ resistor should be tied from the LRCLK to VSS. IF the LRCLK is driving TTL then a 620Ω resistor should be used.

SER0-SER5

These are the serial data lines. Data is transferred on these six lines in 2-word stereo. See the description of the Serial Interface for additional information.

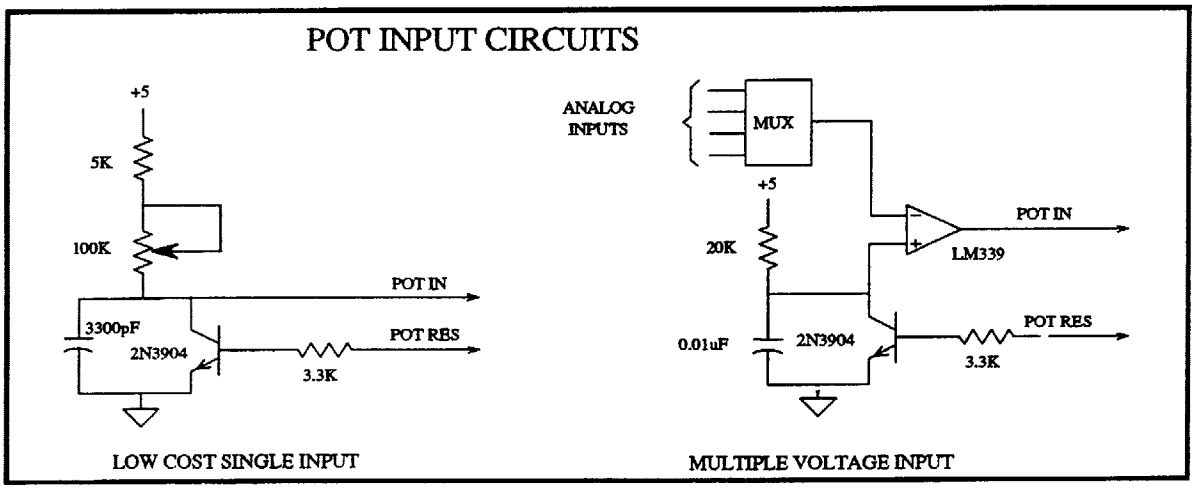
10.4 POTENTIOMETER A/D

POT_IN

This pin is the input to a 10-bit A/D converter for tracking pots and wheels in the system. It's use is described previously in the description of the PAR register.

POT_RES

This pin is a high active output used to reset the external R-C to synchronous the start of the conversion. It is a 50-50 duty cycle clock with a period of 213 counts of the master clock. The following circuits can be used with this converter.



See Section 2.3 for a more complete explanation.

11 ALGORITHMS

The following section describes the data flow and algorithms used in OTTO. To adequately explain the functions which eventually produce the final output, the architecture will be presented in four sections, address generation, sample interpolation, digital filtering and hardware envelopes.

For a more in depth explanation of the theory of digital music and synthesis see *The Musical Applications of Microprocessor* 2nd Ed. by Hal Chamberlin, Hayden Books 1987.

11.1 Address Generation

OTTO uses a technique called "Phase Accumulating Counters" to achieve pitch transposition of a previously sampled waveform. This technique uses an adder, an accumulator and a frequency control word. Each of these component pieces contains an integer and a fractional portion. At each voice time slot, the frequency control word is added to the accumulator and stored back to the accumulator. Consider, for example, that we wish to transpose a sine wave already in memory up one-half octave. This requires that we add to the accumulator the value 1.5 at each accumulation. This calculation can certainly be performed since all the structures have a fractional portion, but the sampled data does not contain a sample 35.5 for instance, only sample 35 or 36. In order to approximate sample 35.5 we must interpolate half way between the two data points contained in samples 35 and 36. Interpolation will be discussed in the next section, and is referred to here since the fractional aspect of the phase accumulating technique requires careful consideration when dealing with the looping.

In order to loop on a waveform the following algorithm is performed.

1. Fetch the Accumulator and put integer portion of the accumulator on external address bus.
2. Add 1 to Accumulator and place on external address bus. This is used for interpolation. The incremented value is not retained.
3. Add Frequency Control Word to Accumulator
4. Subtract Loop End from Accumulator
5. If Loop End > Accumulator then add Frequency Control to Accumulator else add remainder of subtraction in Step 4 to Loop start.

As can be seen the remainder of the subtraction in step 4 is important to keep the phase of the waveform intact when looping and transposing. The counting algorithm presented here is used for all modes of looping except that the roles of the Loop Start and Loop End registers will be swapped depending on the direction of the count.

Note: Since step 5 does a "greater than" compare (>)and not a "greater than or equal to" compare (>=) it is possible for the Accumulator address to be exactly equal to Loop End. If this occurs, on the next sample OTTO will fetch the data at locations Loop End and Loop End + 1. This possibility requires that the Loop End +1 data be set equal to the Loop Start data.

11.2 Sample Data Formats

Sample Data can be stored in memory in two forms. Sample data format is programmable on an individual oscillator basis via a bit in the oscillator control register. In the first mode the data is in 16-bit two's complement format. The second mode is an exponent mantissa format in which the three MSBs are the exponent and the remaining thirteen bits are the mantissa, this method is commonly referred to as μLaw. Data in this format is decompressed before interpolation.

The most useful form of this compression scheme are the 8-bit and 12-bit compressed data formats. Since OTTO does not internally zero the lower bits when the compressed format is used, the system must force the lower data bus to zero when this type of data is read.

In the 8-bit form, the signal will maintain a signal to noise level of -78dB with a THD of -36dB. The 12-bit format will provide a dynamic range of 96dB, equivalent to 16-bit linear, with a THD specification of -60dB.

Algorithm to Create μLaw Data

This program is used to create 8-bit μLAW data from 16-bit linear data. This routine checks for leading "1's or 0's" and removes them. The number of leading "1's or 0's" determines the size of the exponent. The remaining digits are truncated to five bits and right justified to form the mantissa. The exponent is then ORed with the exponent to form the final 8-bit sample

```
done = 0
exp = 7
WHILE (exp > 0 AND done = 0)
  'check to see if first two bits are the same
    IF ( Bit15 = Bit14) THEN
            left shift Sample
             exp = exp - 1              ' decrement exponent
     ELSE
            strip sign bit and truncate Sample to 5 bits
             append Sample to exp
            done = 1          ' compression of this sample complete
    ENDIF
WEND
    IF exp = 0 THEN
            truncate Sample to 5 bits (do not strip sign)
            append Sample to exp
STOP
```

Examples of µLaw

Decimal	16-bit Hex	µLaw Exp	µLaw Mantissa	8-bit µLaw Hex
32767⇒31744	7FFF-7C00	7	31	FF
25599⇒24576	63FF-6000	7	24	F8
17407⇒16384	43FF-4000	7	16	F0
16383⇒15872	3FFF-3E00	6	31	DF
8703⇒8192	21FF-2000	6	16	D0
8191⇒7936	1FFF-1F00	5	31	BF
4351⇒4096	10FF-1000	5	16	B0
4095⇒3968	0FFF-0F80	4	31	9F
2175⇒2048	087F-0800	4	16	90
2047⇒1984	07FF-07C0	3	31	7F
1087⇒1024	043F-0400	3	16	70
1023⇒992	03FF-03E0	2	31	5F
543⇒512	021F-0200	2	16	50
511⇒496	01FF-01F0	1	31	3F
271⇒256	010F-0100	1	16	30
255⇒240	00FF-00F0	0	15	0F
15⇒0	00EF-0000	0	0	00
-32768⇒-31745	8000-83FF	7	0	E0
-17408⇒-16385	BC00-BFFF	7	15	EF
-16384⇒-15873	C000-C1FF	6	0	C0
-8704⇒-8193	DE00-DFFF	6	15	CF
-8192⇒-7937	E000-E0FF	5	0	A0
-4352⇒-4097	EF00-EFFF	5	15	AF
-4096⇒-3969	F000-F07F	4	0	80
-2176⇒-2049	F780-F7FF	4	15	8F
-2048⇒-1985	F800-F83F	3	0	60
-1088⇒-1025	FBC0-FBFF	3	15	6F
-1024⇒-993	FC00-FC1F	2	0	40
-544⇒-513	FDE0-FDFF	2	15	4F
-512⇒-497	FE00-FE0F	1	0	20
-272⇒-257	FEF0-FEFF	1	15	2F
-256⇒-241	FF00-FF0F	0	16	10
-16⇒-1	FF10-FFFF	0	31	1F

11.3 Interpolation

Once two successive samples have been fetched from the sound memory it is necessary to use linear interpolation to approximate a new sample. This approximation is done by performing the following calculation.

SF = S1 + ACCfr * (S2 - S1), where

SF is the new sample,
S1 is first sample fetched,
S2 is the second sample fetched,
ACCfr is the 9 fractional bits of the Accumulator.

The output of the Interpolator is maintained at 18-bits when sent to the filters.

11.4 Digital Filtering

The new sample generated by linear interpolation is ready to be filtered. Each voice in OTTO is passed through four one pole filters. These digital filters each simulate a one pole Butterworth filter. As previously mentioned in the discussion of the filter configuration bits in the CR, filters one and two are fixed as low pass and filters three and four are programmable as either low pass or high pass. Filter results are maintained as 18-bit values with a 16-bit output from filter 4 going to the panning computation.

The block diagrams on the following page shows the actual data path used to perform the filter calculations for each of the filter modes.

The filter coefficients K1 and K2 are used to define the cutoff frequency of the filter. The following set of equations show the set of calculations performed on the sample data stream for each voice. The low pass filter is modeled by:

$Y_n = K * (X_n - Y_{n-1}) + Y_{n-1}$, where

Yn is the new output,
K is cutoff coefficient,
X_n is the input,
Y_{n-1} is the previous output.

The high pass filter is modeled with:

$Y_n = X_n - X_{n-1} + K * Y_{n-1}$, where
Y_n is the new output,
K is cutoff coefficient,
X_n is the input,
X_{n-1} is the previous input.

The four filters are cascaded such that the output of the first is the input to the second and so on.

The coefficients K1 and K2 define the cutoff frequency of the filters. Given a desired attenuation (normally the -3dB point) the value for K can be determined from the following relationship for the low pass filter.

$$K_L = 65535 \times \frac{1-\cos(W)-\sqrt{\cos^2(W) + {}^{2}/_{N2}[1-\cos(W)]-1}}{1-\left({}^{1}/_{N2}\right)}$$, where

K_L is the cutoff coefficient,
$W = 2\pi f/F$, where f=frequency of interest and F is the sampling frequency,
N is the attenuation factor, .707 for -3dB.

A similar relationship can be developed for the high pass filter.

$$K_H = 65535 \times \left\{\cos(W)-.5-\sqrt{\cos^2(W) + {}^{2}/_{N2}[1-\cos(W)]-1}\right\}$$, where

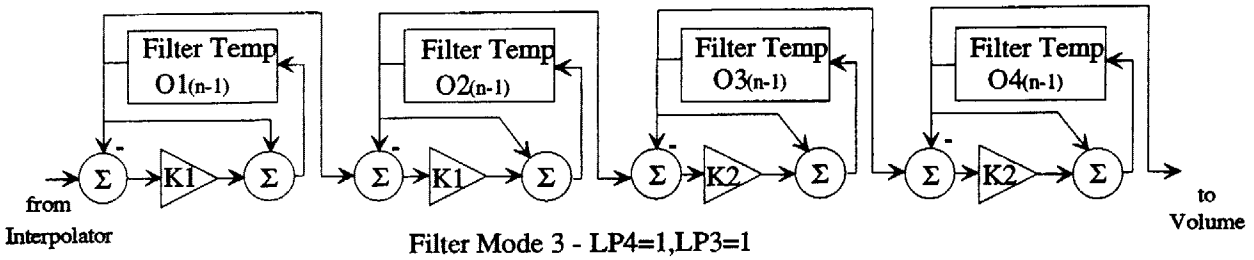
K_H is the cutoff coefficient,
$W = 2\pi f/F$, where f=frequency of interest and F is the sampling frequency,
N is the attenuation factor, .707 for -3dB.

The most useful range of a high pass filter is generally below 4kHz. In order to maximize the resolution of the filter in that range an offset of .5 has been added to the K_H coefficient. This offset means the highest cutoff frequency achievable is approximately 8000Hz. for one high pass pole.

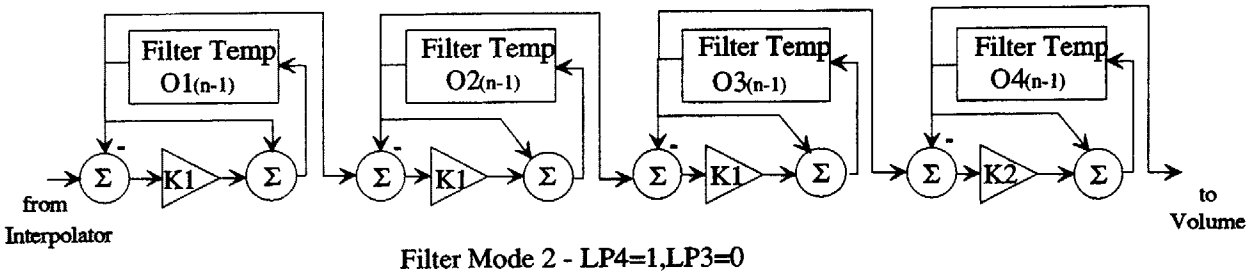
Remember that the equations presented here are for one pole only, and the value for the attenuation factor N must be scaled for the number of poles.

# of Poles	N
1	.707
2	.84
3	.89
4	.91

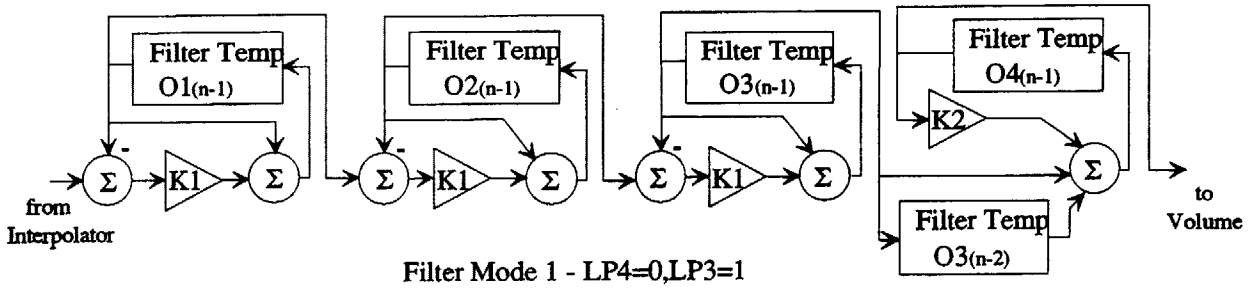
Filter Modes Block Diagram



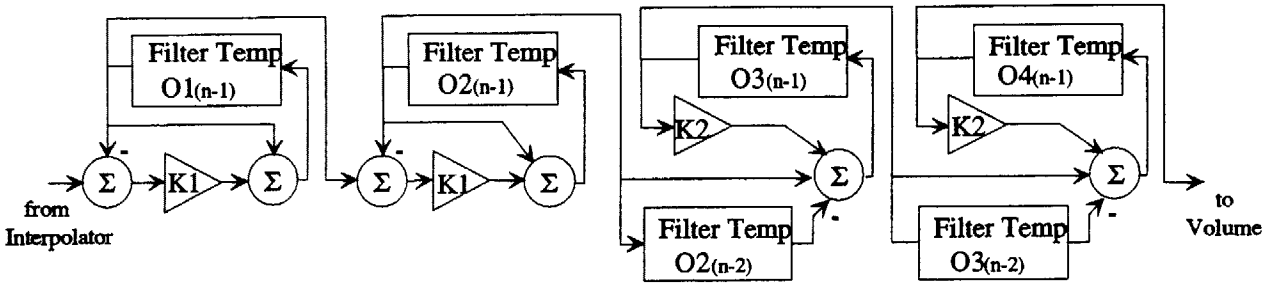
Filter Mode 3 - LP4=1,LP3=1



Filter Mode 2 - LP4=1,LP3=0



Filter Mode 1 - LP4=0,LP3=1



Filter Mode 0 - LP4=0,LP3=0

11.5 Hardware Envelopes

Hardware envelopes are implemented on left volume LVOL, right volume RVOL, filter coefficient K1 and filter coefficient K2. The algorithm is as follows.

The ECOUNT value will be checked upon reading the oscillator data, and immediately before updating the oscillator. If it is zero at either time, the update of volume and filter coefficient registers will be aborted.

The addition operation shown below is a signed addition with saturation. A special mode of operation for the filter envelopes using an internal counter (FILTCOUNT) causes the above algorithm to execute on every eighth sample cycle for slow moving envelopes if the SLOW bit is set.

Hardware Envelope Algorithm

```
if ECOUNT ≠ 0
        LVOL = LVOL + sign_extended(LVRAMP)
        RVOL = RVOL + sign_extended(RVRAMP)
        if ( K1SLOW = 0 ) or (FILTCOUNT = 0)
                K1 = K1 + sign_extended(K1RAMP)
        endif
        if ( K1SLOW = 0 ) or (FILTCOUNT = 0)
                K2 = K2 + sign_extended(K2RAMP)
        endif
        ECOUNT = ECOUNT - 1
endif
FILTCOUNT = FILTCOUNT + 1
```

The register involved in the hardware envelope algorithm are:

REGISTER	# of Bits	Notes
ECOUNT	9	common to all four envelopes
LVOL	16	12 MSB's used in volume multiply
LVRAMP	8	sign extended for multiply
RVOL	16	12 MSB's used in volume multiply
RVRAMP	8	sign extended for multiply
K1	16	12 MSB's used in filter multiply
K1RAMP	8	sign extended for multiply
K2	16	12 MSB's used in filter multiply
K2RAMP	8	sign extended for multiply

11.6 Stereo Panning

The filter outputs go through a stereo pan calculation in which the signal is multiplied by left and right volume values to split into left and right signals. This allows panning with the same resolution as volume adjust. The volume values are contained in registers as a 4 bit exponent and a 8-bit mantissa. The computation is performed as follows:

1. The 16-bit signal is multiplied by the value 1MMMMMMMM where M's represent the 8-bits of the mantissa.

2. The 20 MSB's of the result of step 1 are then right shifted by the value 15 - exponent.

The result of the stereo pan calculation will be assigned to one of six channels based on the three voice dependent channel assign bits (CA2-CA0). These six channels are implemented as twelve accumulating registers (left and right for each of six channels) and will sum signals during a complete sample cycle.

11.7 MORE on OTTO Hardware Envelopes

OTTO Ramps: Why they are the way they are.

The MIDI model of electronic musical requires that every sound must respond to real time control. At the least, a sound must respond to volume and pitch bend messages as they arrive from MIDI. This means that is not appropriate to pre-define the entire amplitude envelope shape in a set a registers inside the chip. Instead, a microprocessor will feed incremental control parameters to the chip at a sample rate of approximately 100Hz.

Typically the controlling microprocessor will generate software envelopes. The envelope data is then scaled and combined with other control information, such as master volume, panning and LFO modulation. The complexity of these calculations will vary with the particular voice architecture implemented. The results of these calculations are the instantaneous values for each voice's frequency, filter cutoff, and right/left volumes. These values are usually recalculated every 10 to 20 milliseconds.

The ramp generators in OTTO are used to smooth out the filter cutoff and volume control signals. Large jumps in the FC and volume will cause audible glitches in the signal. The ramp generates a smoothly changing signal from one value to the next.

OTTO Ramps: Theory of Operation.

Every sample period the ramp generator calculates the next step of the ramp. It does this by adding a small negative or positive number to the current value. There is clipping protection built in so that the ramp does not "wrap" over the top when it hits the maximum value, or when it tries to go below zero in the case of a negative going ramp.

The COUNT register controls how many times the increment will be added. When the count decrements to zero then the ramps will freeze at their current value.

The coefficients for the filters, K1 and K2, have a non linear response. This means that the steps at the bottom of the range are fairly coarse. To adjust for this, the filter ramp has a special mode to allow for very slow ramps.

OTTO Ramps: In Practice.

Choose a software update period for the system. In general, shorter periods are better, but require more CPU time. Again, the range of 10 to 20 milliseconds is usual. ENSONIQ uses 12 msec. A good update rate for a video game system would be 16.6 milliseconds, the same as the video update rate.

Compute the number of samples in one update period. This will be the number of steps in the ramp.

Number of Steps = Sample Rate × Update Period

For example, 31250 Hz × .012 seconds = 375 steps.

Another example 31250 Hz × .0166 seconds = 518 steps.

(Note: In this case, you will have to settle for 511 steps in the ramp, because this is the largest ramp available)

When a voice starts up, the voice software must calculate the initial value for the amplitude and filter cutoff frequency values, and write these into the chip. The CPU must then calculate the FUTURE amplitude and fc values - what they should be after the first update period.

Compute the increment value for the ramp. The increment should be the difference between the current and the future value for the ramp, divided by the number of steps.

Increment = (Future Current - Current Value) / Number of Steps

(Note: the increment register is left justified, which might help eliminate any divide or shift operation in the case of 512 steps. Otherwise it is generally more efficient to multiply by 1/Number-of-steps than to divide.)

To write the ramp increments into the chip:

1. Stop the ramp by writing a zero into the COUNT register.
2. Write all four increment values, LVRAMP, RVRAMP, K1RAMP, K2RAMP.
3. Start the ramps by writing the number of steps into the COUNT register.

12 SERIAL OUTPUT AND PLAYBACK

Once a cycle of the total number of voices has completed, the results of the channel accumulations are latched into shift registers and transmitted out through the serial port for use by external DSP's or D/A's. The accumulators are then cleared to begin the next voice cycle.

The accumulator is 23 bits wide of which 3 bits are guard bits.

The serial clocks are bit-programmable to input or output on an individual basis.

Because of the great diversity of definitions for serial clock timings among the commercially available D/A's and A/D's, the best approach to this problem is to make the serial interface fully programmable. This will make the interface flexible instead of locking the chip into a hardwired configuration which may or may not satisfy current and future needs. Programmability is achieved through a BCLK counter and the following registers.

WCLK_ST	Defines the start of WCLK and serial data.
WCLK_END	Defines the end of WCLK and serial data.
LRCLK_END	Defines the end of LRCLK.

If OTTO is driving LRCLK, it will assert when all voices have been accumulated into the channel registers. This occurs when the internal oscillator counter wraps back to zero. This will reset the BCLK counter. The position and duration of WCLK and DATA will be determined by comparing the values of WCLK_ST and WCLK_END to the counter. The falling edge of LRCLK is defined by LRCLK_END. This gives full flexibility on the separation of right and left channels, the justification of the data transfer with respect to LRCLK transitions, and the number of bits of data transfer via adjusting the start and end of WCLK and the data transfer window. Since the counter will reset on the falling edge of LRCLK as well, the right data transfer will be defined the same as the left via WCLK_ST and WCLK_END.

Separate tristate control of BCLK, WCLK, and LRCLK is provided. Therefore, in the event that a chip which did not provide WCLK had to be master of the transfer via LRCLK, OTTO could still generate WCLK for an external chip requiring such a signal.

OTTO decides when to output data based solely on the WCLK_ST and WCLK_END registers. It does not watch the external WCLK signal for making this determination, therefore the WCLK_ST and WCLK_END should always be setup, even when OTTO is not supplying the external WCLK signal.

Figure 16.5 illustrates serial timings programmed for left justified 16- or 18-bit data. In this example, W_ST=1, LR_END=32, and W_END=17 or 19 depending on the word length.

13 HOST INTERFACE.

The host accesses OTTO through a dedicated host interface consisting of 8 data lines and 6 address lines. Processor interaction with chip registers will take place according to the following rules:

1. All registers will appear as 32-bit entities addressed by the upper four address lines. The 2 lowest address lines will act as byte selects.

2. Writes of registers will occur such that bytes other than byte 3 will be latched in temporary registers until such time that byte 3 is addressed for writing. At this time the register will be modified in its entire width.
3. Register reads will occur as 32-bit operations such that addressing byte zero will cause a 32-bit read to occur with bytes 1, 2, and 3 being latched. A read operation addressing bytes 1, 2, and 3 will access the temporary latch rather than the contents of the register.

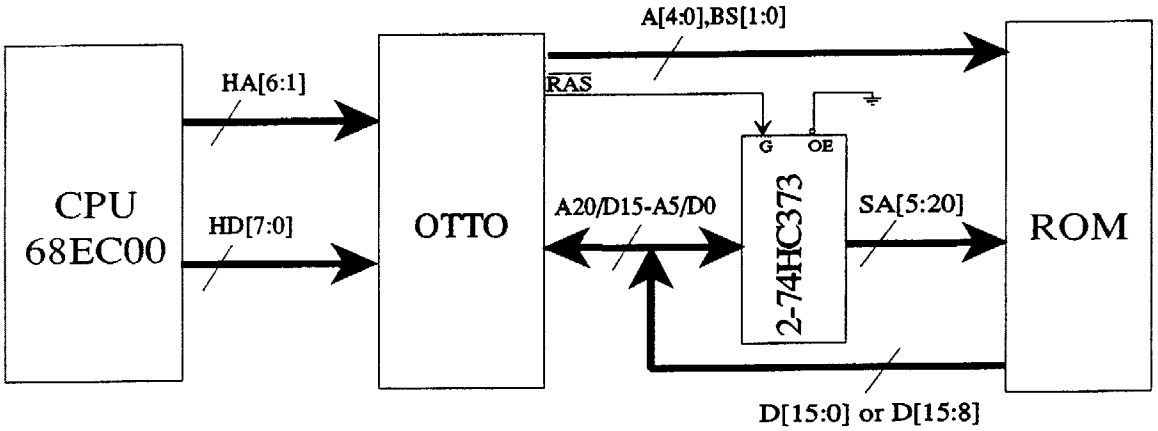
DMA access to memory will occur as 16-bit operations only when memory cycles become available. In a single OTTO system, DMA slots are available every other memory cycle. In a dual OTTO system, the two OTTO's alternate accesses on every memory cycle apparently leaving no time for DMA operations. DMA has been provided by recognizing when stopped oscillators occur in the master OTTO. If an oscillator is stopped its volume is forced to zero and therefore its samples are not needed. The memory cycles are allocated to DMA. Memory access should be requested via the MSB (Memory Select) pin of the master OTTO. External latches are required for address and data (see Host Block Diagrams). The following rules apply:

1 On CPU writes, the address and upper byte of data will be latched external to OTTO. The lower byte of data will be latched in OTTO, and DTACKB will be asserted. When a sound memory cycle becomes available, the memory write will occur. Attempts to write memory again, before the first write has been completed, will result in the host bus being wait-stated, until the latches are free.
2 On CPU reads, the host bus will be wait-stated until a memory cycle becomes available for completion of the read.
3 The interface to the host is fully asynchronous with processor data and address being latched at the buffers and cycle duration being controlled by CSB, MSB, and DTACKB.

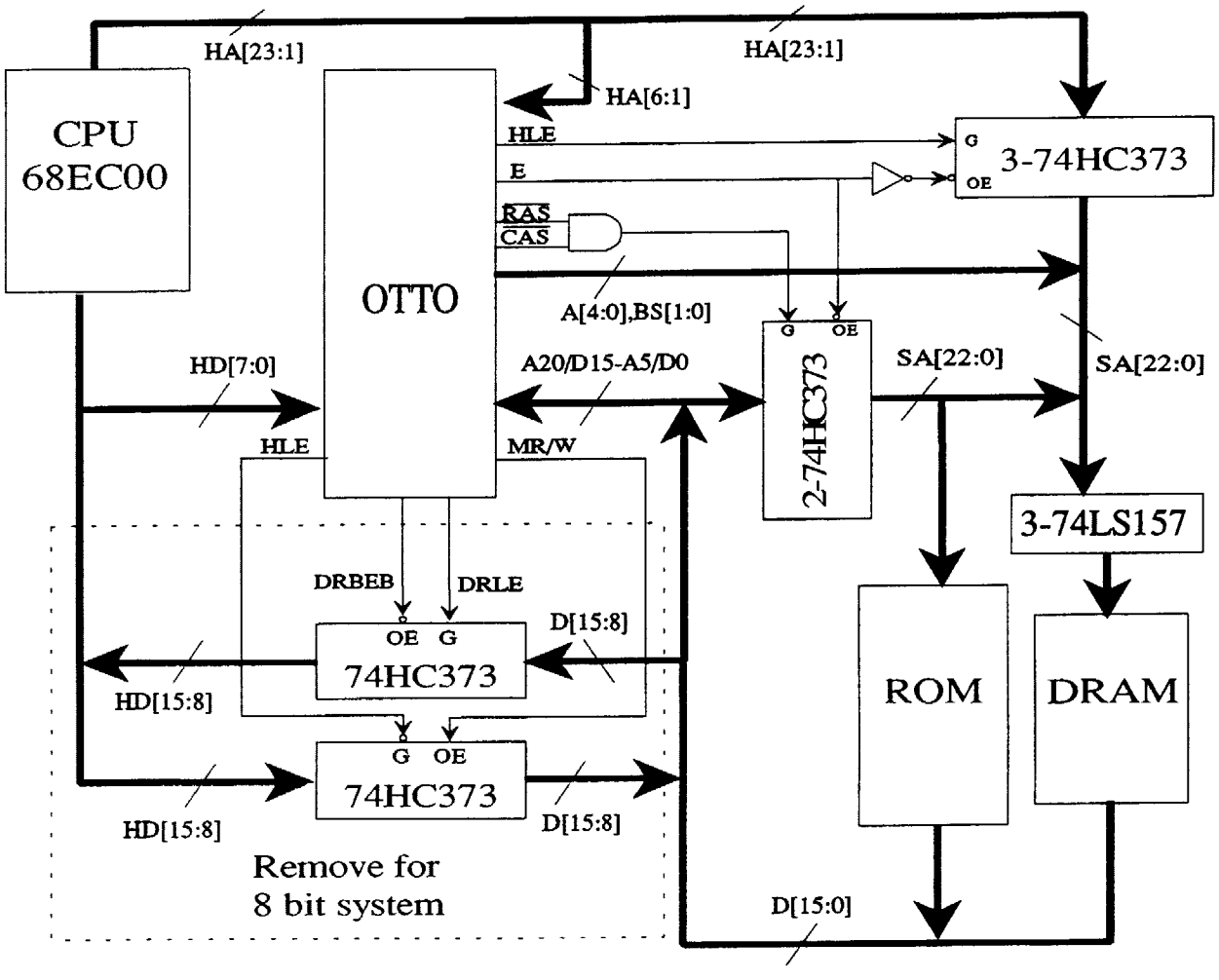
13.1 Host Interface Block Diagrams

The following block diagrams show the basic architecture used to interface the OTTO chip in a system. The simplest configuration is ROM based. In the Sound ROM only system the CPU communicates only with OTTO and the sounds to be played are stored in ROM.

In a RAM based system, the CPU must access the DRAM on the Sound Memory Bus. The communication between the CPU and the RAM must be synchronized to the OTTO timing. OTTO provides all the signal necessary for CPU DMA to the Sound Memory.



8 OR 16 BIT ROM BASED OTTO SYSTEM



16 BIT RAM AND ROM OTTO SYSTEM

14 INTERRUPT HANDLING

An interrupt can be caused by any active voice in OTTO. A voice will request interrupt servicing when the interrupt enable bit has been set and the accumulator has reached the loop end point (loop start if the direction bit is set). An interrupt will be issued by a voice regardless of the state of the loop mode bits when the accumulator reaches the loop end.

When an interrupt has been requested, the interrupt bit (bit 7 in the Control Register) is set, the voice number is latched into the Voice Interrupt Vector register and bit 7 of the Voice Vector register is cleared low. When the processor reads the Voice Vector register, bit 7 of the Voice Vector register is set high and when the voice which caused the interrupt is next processed, bit 7 of its Control Register is cleared.

If a voice has reached an interrupt condition and the Voice Vector already contains information from another voice, the new Interrupt will be stacked. This stacking occurs automatically since the interrupt bit in the Control Register of the voice will be set when the interrupt condition occurs. Eventually the processor reads the Voice Vector clearing the old interrupt vector information and the new vector will be placed in the register when the new voice is again processed. Note this ability allows the processor to force an interrupt from a voice simply by setting the interrupt enable bit and the interrupt bit of a particular voice.

15 ELECTRICAL SPECIFICATIONS

14.1 Maximum Ratings

Rating	Symbol	Value	Units
Supply Voltage	VDD	-0.3 to 7	V
Input Voltage	VIN	-0.3 to 7	V
Operating Temperature	TA	0 to 70	C
Storage Temperature	TSTG	-55 to 150	C

14.2 DC Electrical Characteristics

VDD = 5.0V ± 5%, VSS = 0V, TA = 0°C to 70°C

Characteristic	Symbol	MIN	MAX	Units
Input High Voltage	VIH	2.2	VDD	V
Input Low Voltage	VIL	-0.3	0.7	V
Input Leakage Current @VDD	IIN	-	10	uA
Hi-Z leakage @2.4V/0.5V	ITSI	-	20	uA
Output High Voltage IOH @ -400uA (except DTACKB, IRQB)	VOH	-	2.4	V
Output Low Voltage IOL @ 4mA	VOL	0.5	V	
Power Dissipation	PD	-	400	mW

16 TIMING DIAGRAMS

AC ELECTRICAL SPECIFICATION - SEE FIGURES 16.1 TO 16.5

Operating Conditions: 0° to 70° @ 16Mhz Input Clock Frequency

Num.	Characteristic	Symbol	Min	Typ	Max	units
-	Input Clock Frequency	CLKFr	8.0	16.0	16.9	Mhz
1	Clkin to E fall delay	EFD	15	20	28	ns
2	Clkin to E rise delay	ERD	15	20	28	ns
3	Clkin to RAS delay	CDRAS	13	18	25	ns
4	E transition to RAS fall delay	ERASD	60	65	70	ns
5	RAS high width	RASHW	125	130	135	ns
6	RAS to AMUX delay	RAMUXD	28	32	36	ns
7	E transition to AMUX delay	EAMUXD	95	100	105	ns
8	AMUX to CAS delay	AMUXCD	28	32	36	ns
9	CAS high width	CASHW	125	130	135	ns
10	CS, R/W, HA, HD, MS to E step time	CSE	25	-	-	ns
11	DTACK, DRE hold after CS high	DTACKH	-	12	20	ns
12	DTACK to E delay	DTACKE	130	140	150	ns
13	R/W hold time	RWH	150	-	-	ns
14	Host Address (HA) hold time	HAH	150	-	-	ns
15	Host Data (HD) hold time	HDH	150	-	-	ns
16	Host Data (HD) access time	HDACC	-	150	180	ns
17	HD[7:0] hold after CS high	HDCSH	10	15	30	ns
18	A[4:0], BS[1:0] Address Output Delay	ALOD	10	15	25	ns
19	A[4:0], BS[1:0] Address Output Hold	ALOH	-	15	20	ns
20	A[20:5] Address Out Delay	AHOD	-	45	55	ns
21	A[20:5] Address Out hold after CAS	AHOH	10	14	20	ns
22	D[15:0] Sound Data to E set up time	DSU	35	-	-	ns
23	D[15:0] Data in hold time	DH	10	-	-	ns
24	DRLE Data Latch Enable delay time	DRLED	-	150	160	ns
25	DRLE Data Latch Enable hold time	DRLEH	-	6	12	ns
26	D[7:0] thru OTTO to HD[7:0] delay	DHDD		18	25	ns
27	HEN on delay	HENon	-	17	25	ns
28	HEN off delay	HENoff	-	17	25	ns
29	HLE on delay	HLEon	-	17	25	ns
30	HLE pulse width	HLEPW	110	120	130	ns
31	MR/W enable delay	MR/W	-	22	30	ns
32	MR/W hold after E	MR/WH	-	30	37	ns
33	D[7:0] Data out delay after E	DDE	-	40	50	ns
34	D[7:0] Data out hold	DOH	12	18	25	ns

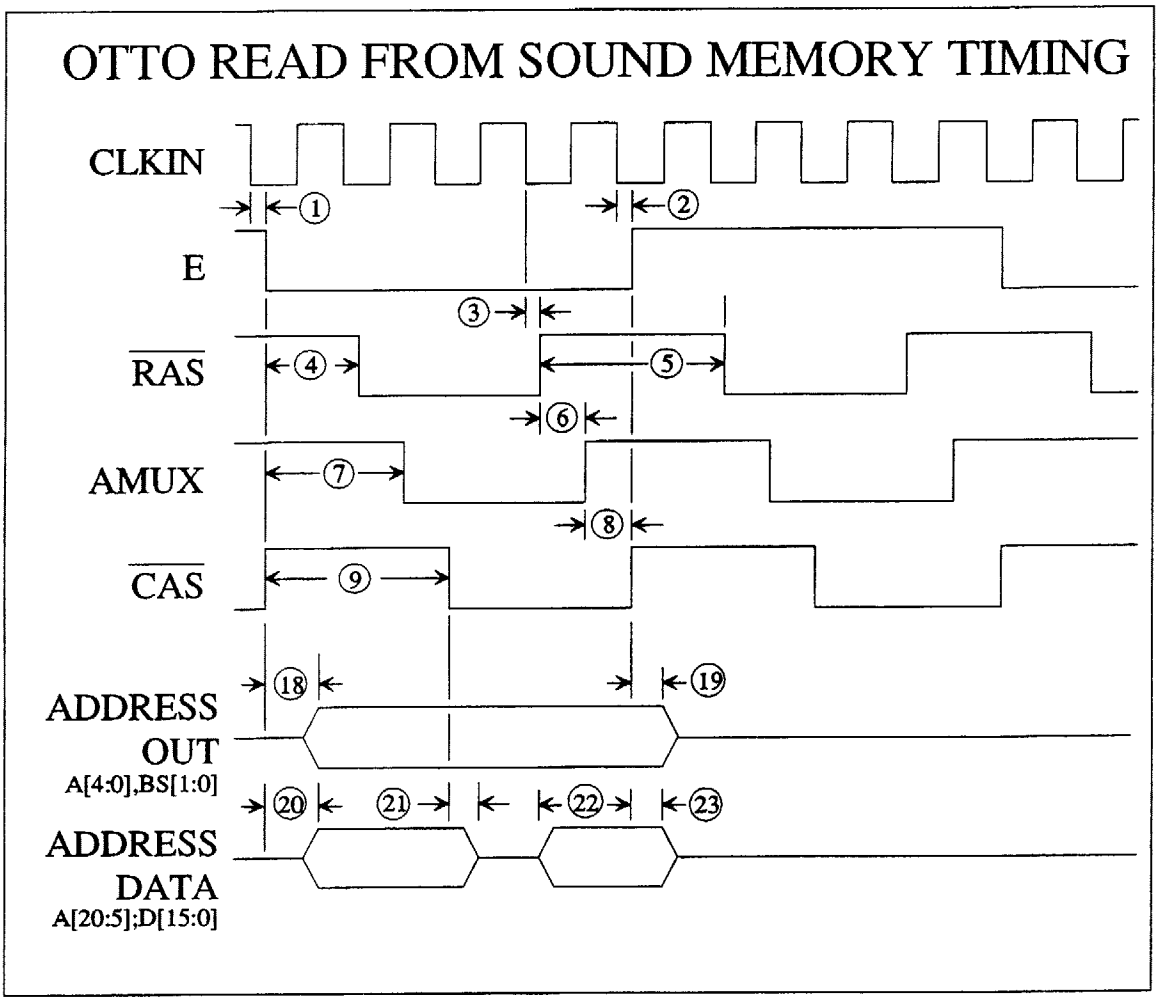

OTTO READ FROM SOUND MEMORY TIMING
CLKIN
E
RAS
AMUX
CAS
ADDRESS OUT
A[4:0],BS[1:0]
ADDRESS DATA
A[20:5];D[15:0]
1
2
3
4
5
6
7
8
9
18
19
20
21
22
23

Figure 16.1

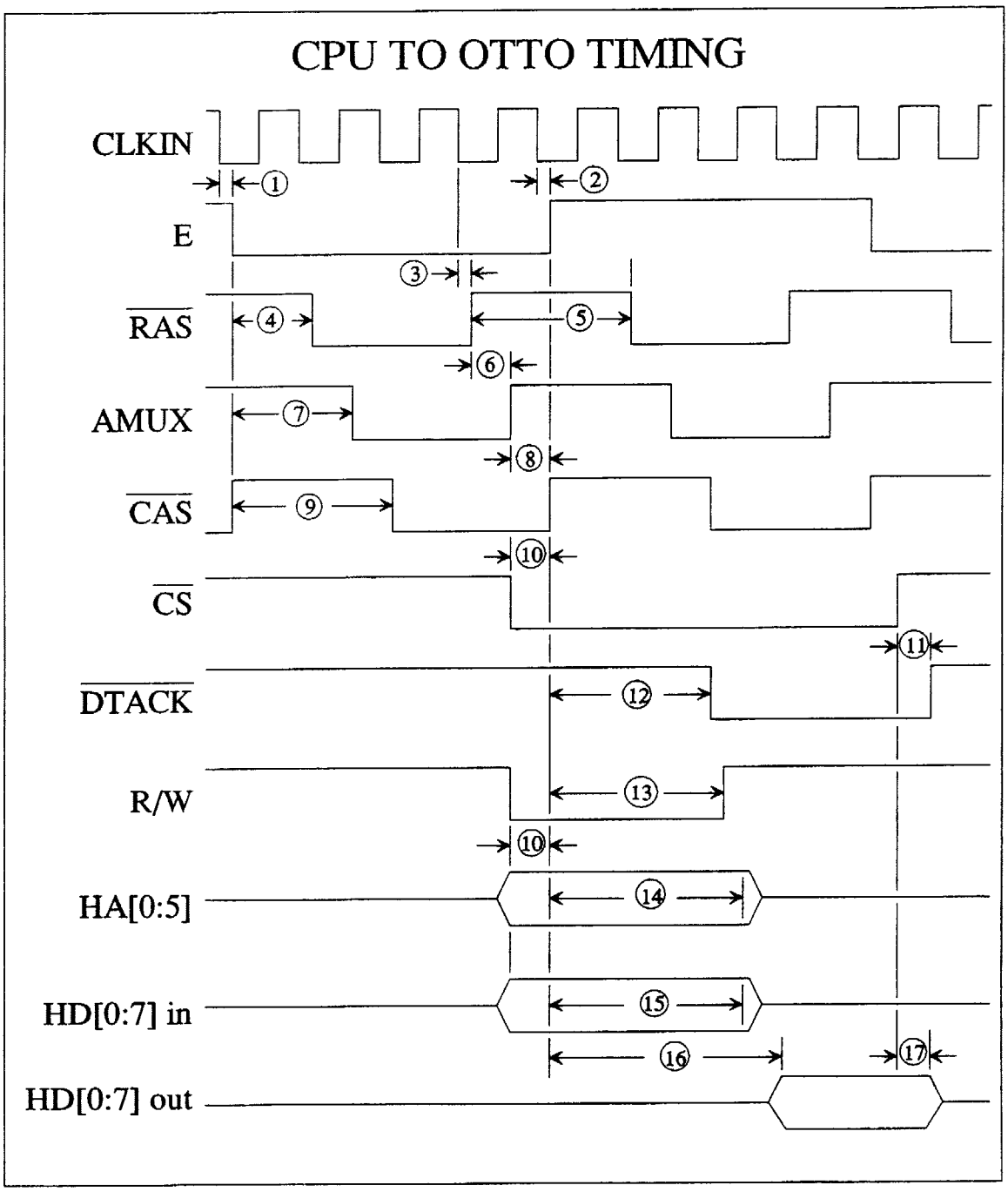

CPU TO OTTO TIMING
CLKIN
E
RAS
AMUX
CAS
CS
DTACK
R/W
HA[0:5]
HD[0:7] in
HD[0:7] out
1
2
3
4
5
6
7
8
9
10
11
12
13
10
14
15
16
17

Figure 16.2

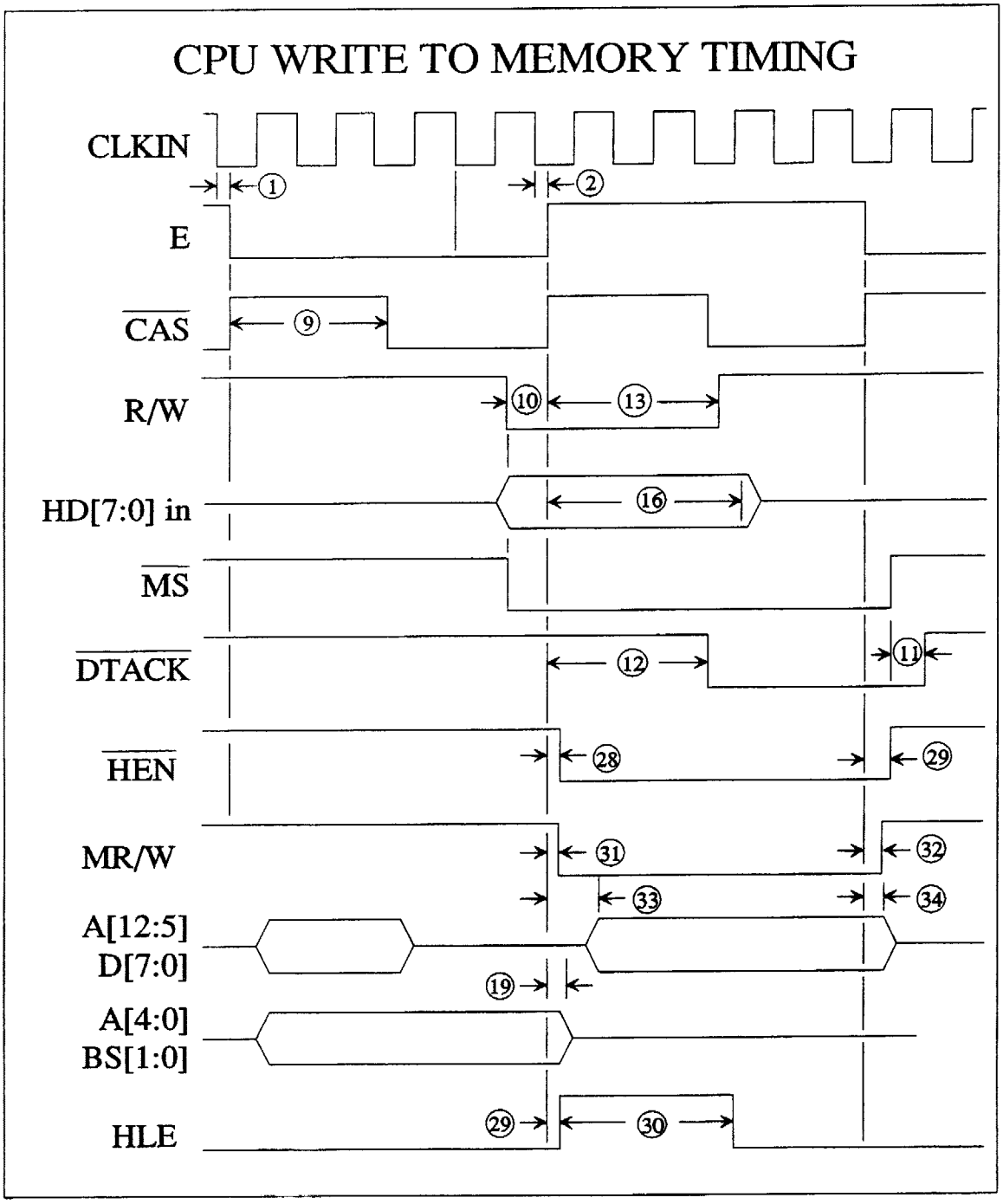

CPU WRITE TO MEMORY TIMING
CLKIN
E
CAS
R/W
HD[7:0] in
MS
DTACK
HEN
MR/W
A[12:5]
D[7:0]
A[4:0]
BS[1:0]
HLE
1
2
9
10
13
16
12
11
28
29
31
32
33
34
19
29
30

Figure 16.3

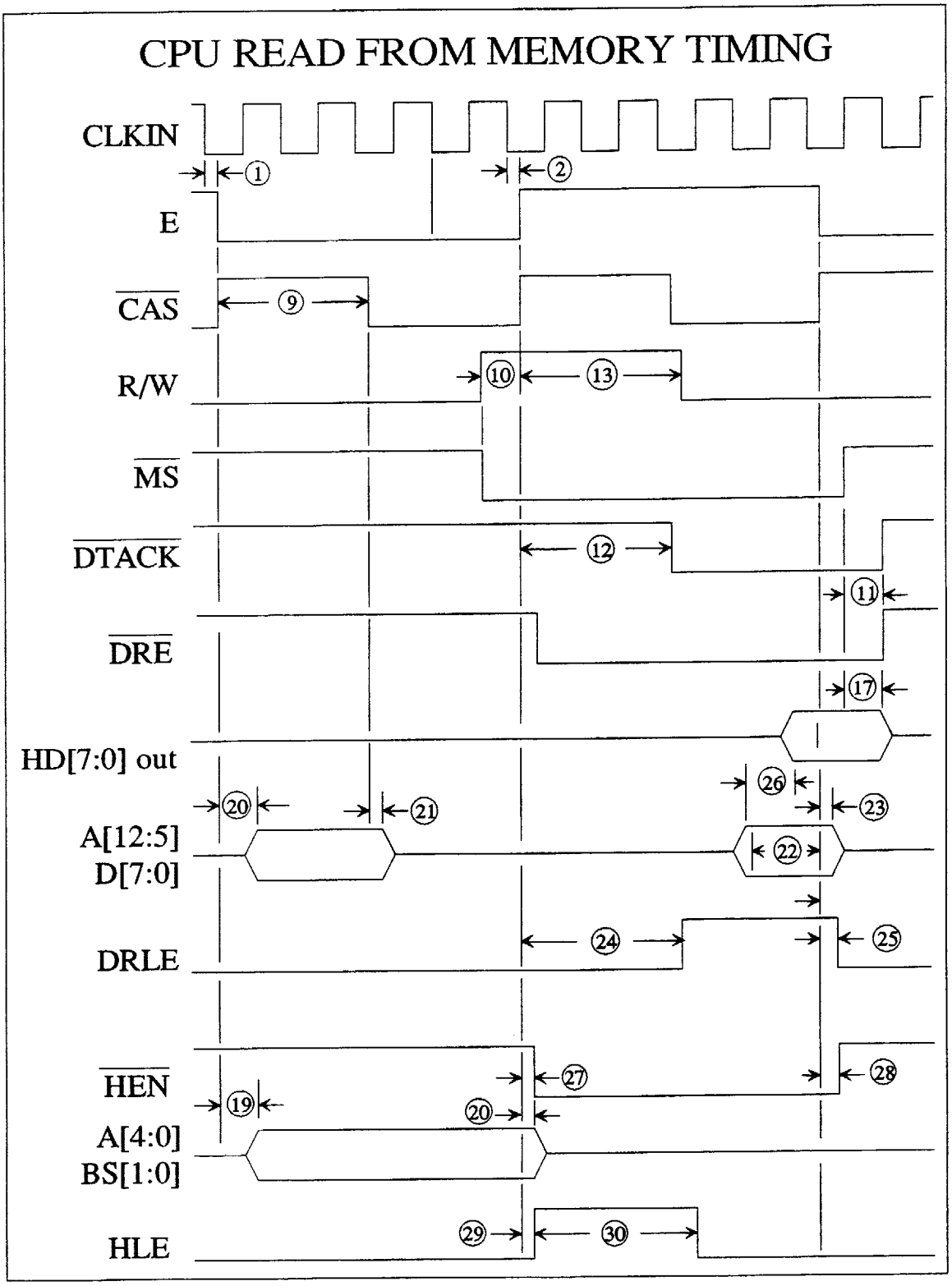

CPU READ FROM MEMORY TIMING
CLKIN
E
CAS
R/W
MS
DTACK
DRE
HD[7:0] out
A[12:5]
D[7:0]
DRLE
HEN
A[4:0]
BS[1:0]
HLE
1
2
9
10
13
12
11
17
20
21
26
23
22
24
25
27
28
19
20
29
30

Figure 16.4

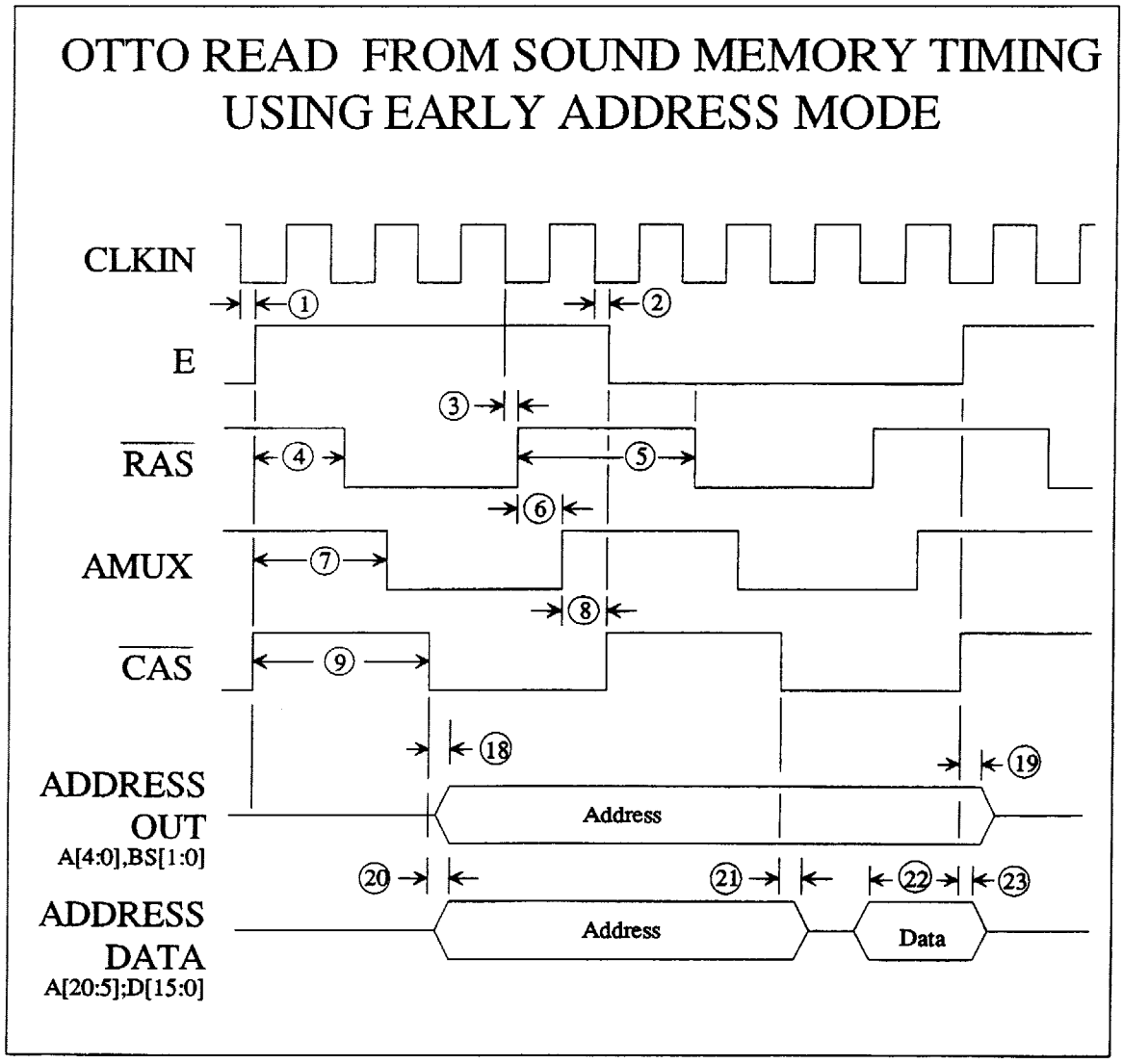

OTTO READ FROM SOUND MEMORY TIMING
USING EARLY ADDRESS MODE
CLKIN
E
RAS
AMUX
CAS
ADDRESS OUT
A[4:0],BS[1:0]
ADDRESS DATA
A[20:5];D[15:0]
1
2
3
4
5
6
7
8
9
18
19
20
21
22
23
Address
Address
Data

Figure 16.5

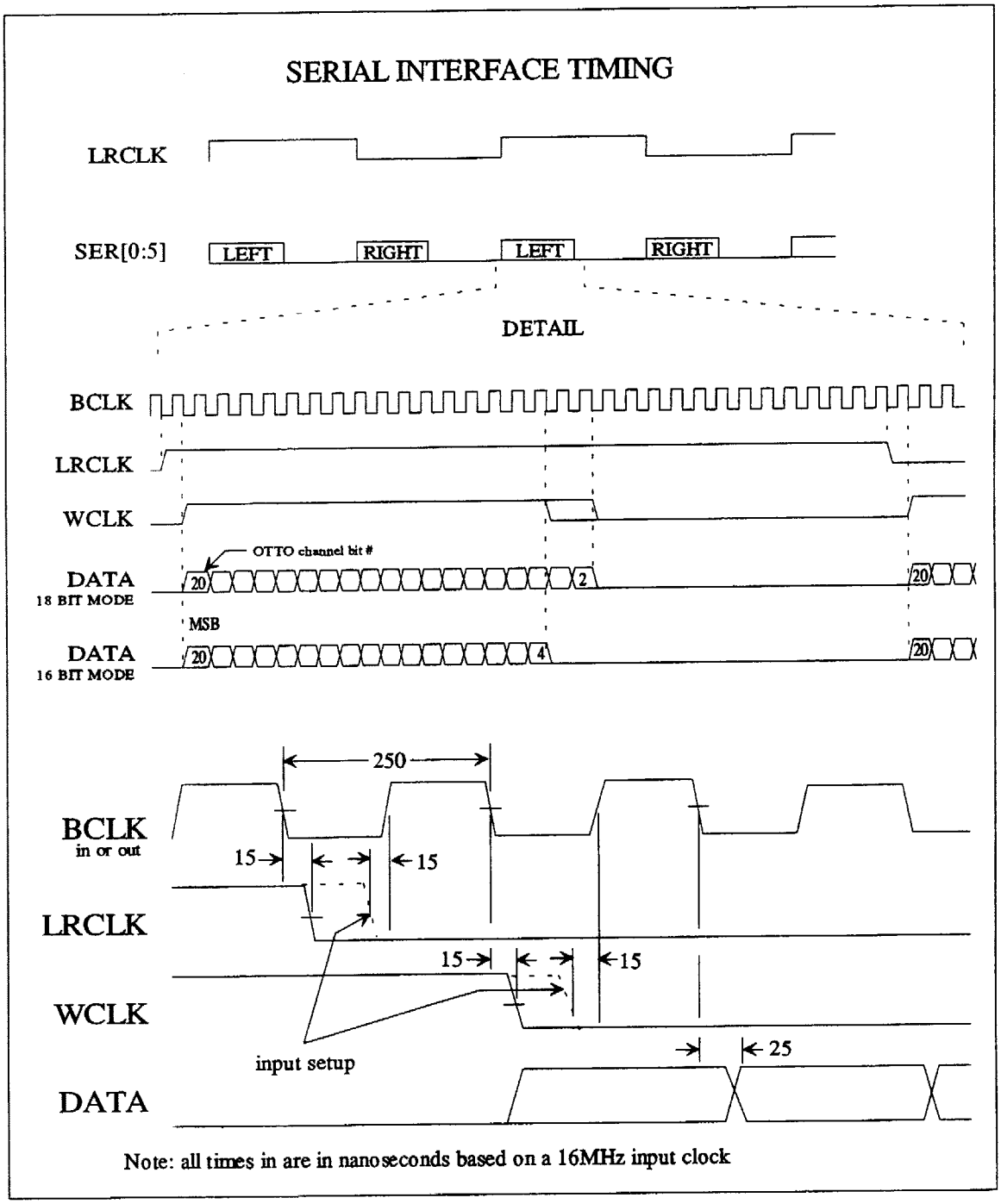

SERIAL INTERFACE TIMING
LRCLK
SER[0:5]
LEFT
RIGHT
LEFT
RIGHT
DETAIL
BCLK
LRCLK
WCLK
OTTO channel bit #
DATA
18 BIT MODE
20
2
20
MSB
DATA
16 BIT MODE
20
4
20
250
BCLK
in or out
15
15
LRCLK
15
15
WCLK
input setup
25
DATA
Note: all times in are in nanoseconds based on a 16MHz input clock

Figure 16.6

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International Manufacturer's Reps

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Minnesota, Iowa, North and South Dakota, Wisconsin	High Tech 4801 W. 81st Street, Suite 115 Bloomington, MN 55437	(P) 612-844-9933 (F) 612-844-9930
Northern California	Magna Sales, Inc. 3333 Bowers Avenue, Suite 251 Santa Clara, CA 95054	(P) 408-727-8753 (F) 408-727-8573
Southern California	SC Cubed 17862 17th Street, Suite 207 Tustin, CA 92680	(P) 714-731-9206 (F) 714-731-7801
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Florida	PSA, Inc. 3537 Lakeview Blvd. Delray Beach, FL 33445	(P) 407-498-2029 (F) 407-499-7987

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